EE 435

Lecture 23

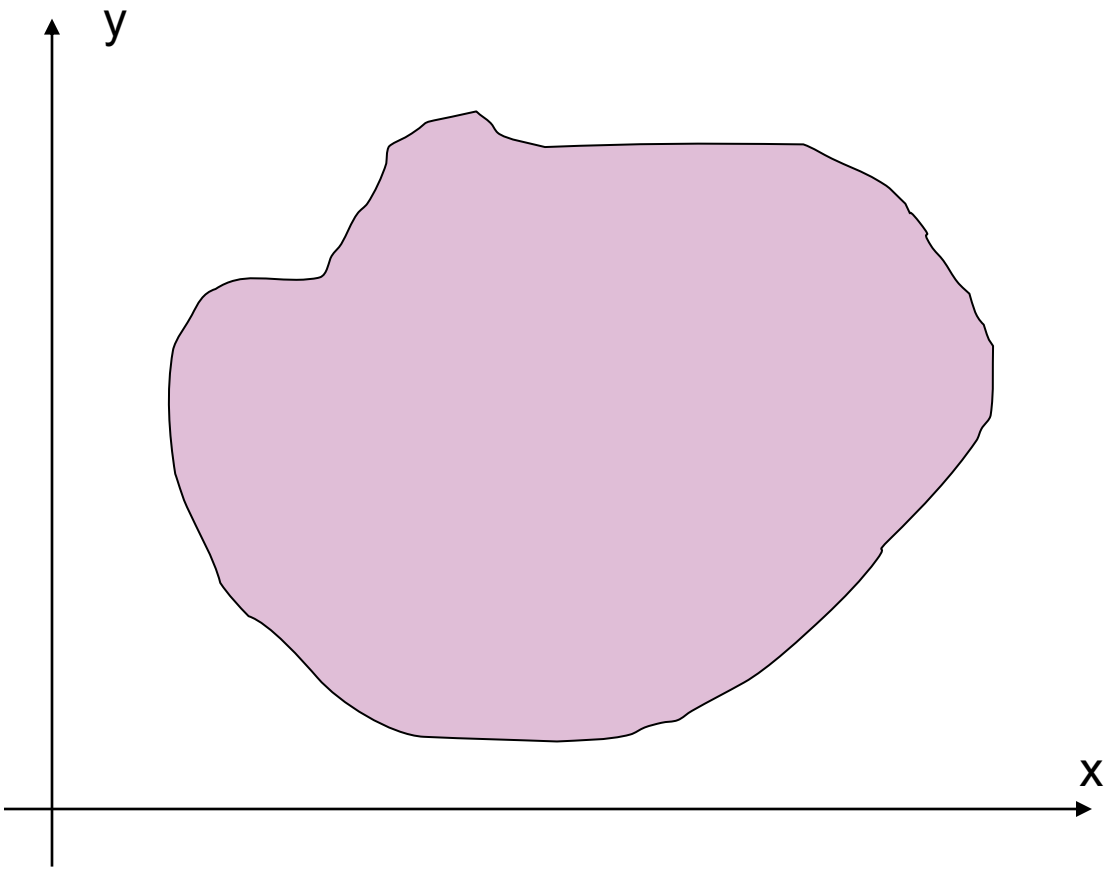
Offset voltage : Gradient Effects

Layout of Analog Circuits (brief)

Common Mode Feedback Circuits

Review from last lecture

Model Parameter Variation



$$p_{EQ} = \frac{1}{A}\int_{A} p(x,y)\,dx\,dy$$

Review from last lecture

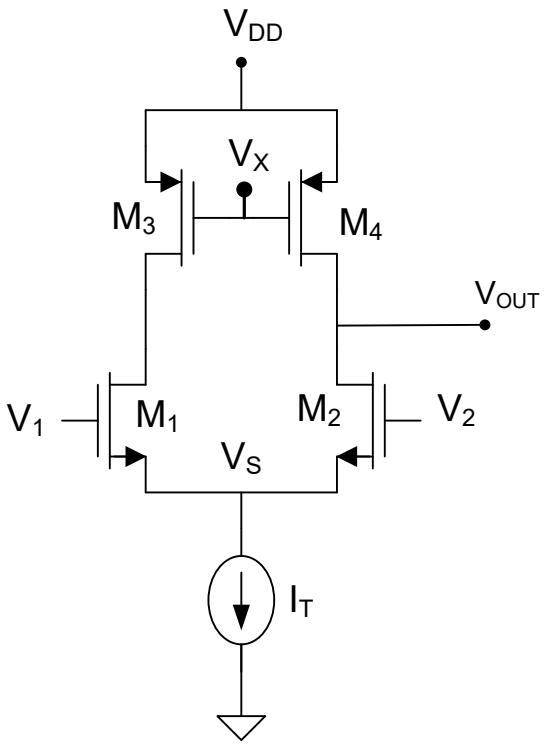
Random Offset Voltages

Correspondingly:

$$\sigma^2_{V_{OS}} = 2\left[\frac{A^2_{VTOn}}{W_n L_n} + \frac{\mu_p}{\mu_n}\frac{L_n}{W_n L_p^2}A^2_{VTOp} + \frac{V^2_{EBn}}{4}\left(\frac{1}{W_n L_n}A^2_{\mu_n} + \frac{1}{W_p L_p}A^2_{\mu_p} + A^2_{COX}\left[\frac{1}{W_n L_n} + \frac{1}{W_p L_p}\right] + 2A^2_L\left[\frac{1}{W_n L_n^2} + \frac{1}{W_p L_p^2}\right] + A^2_w\left[\frac{1}{L_n W_n^2} + \frac{1}{L_p W_p^2}\right]\right)\right]$$

which again simplifies to

$$\sigma^2_{V_{OS}} \cong 2\left[\frac{A^2_{VTO\,n}}{W_n L_n} + \frac{\mu_p}{\mu_n}\frac{L_n}{W_n L_p^2}A^2_{VTO\,p}\right]$$



Note these offset voltage expressions are identical!

Review from last lecture

Random Offset Voltages

$$\sigma^2_{V_{OS}} \cong 2\left[\frac{A^2_{VTO\,n}}{W_n L_n} + \frac{\mu_p}{\mu_n}\frac{L_n}{W_n L_p^2} A^2_{VTO\,p}\right]$$

This expression has somewhat peculiar coefficients. The first term on the right is dependent upon the reciprocal of the area of the n-channel device but the corresponding coefficient on the second term on the right appears to depend upon the dimensions of both the n-channel and p-channel devices. But this can be rewritten as

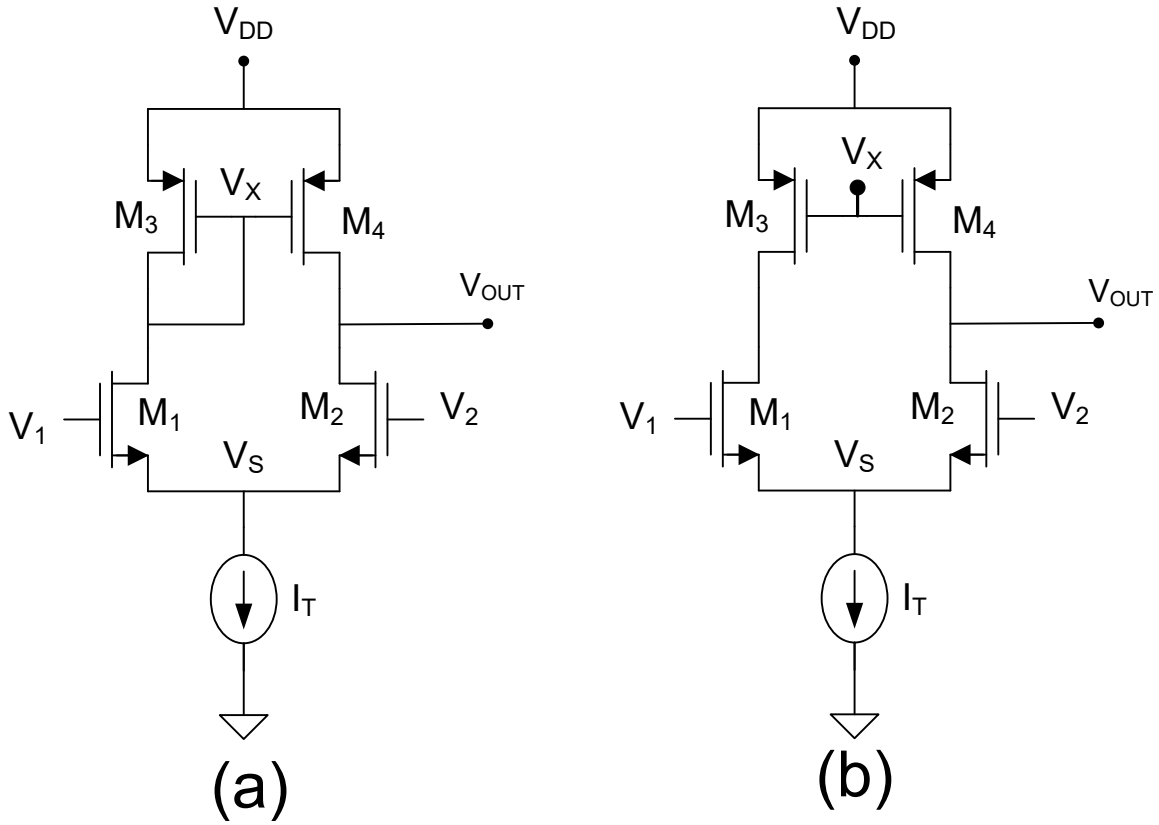
$$\sigma^2_{V_{OS}} \cong 2\left[\frac{A^2_{VTO\,n}}{W_n L_n} + \left(\frac{V_{EB\,n}}{V_{EB\,p}}\right)^2 \frac{A^2_{VTO\,p}}{W_p L_p}\right]$$

The dependence of the variance on the area of the n-channel and p-channel devices is more apparent when written in this form.

Review from last lecture

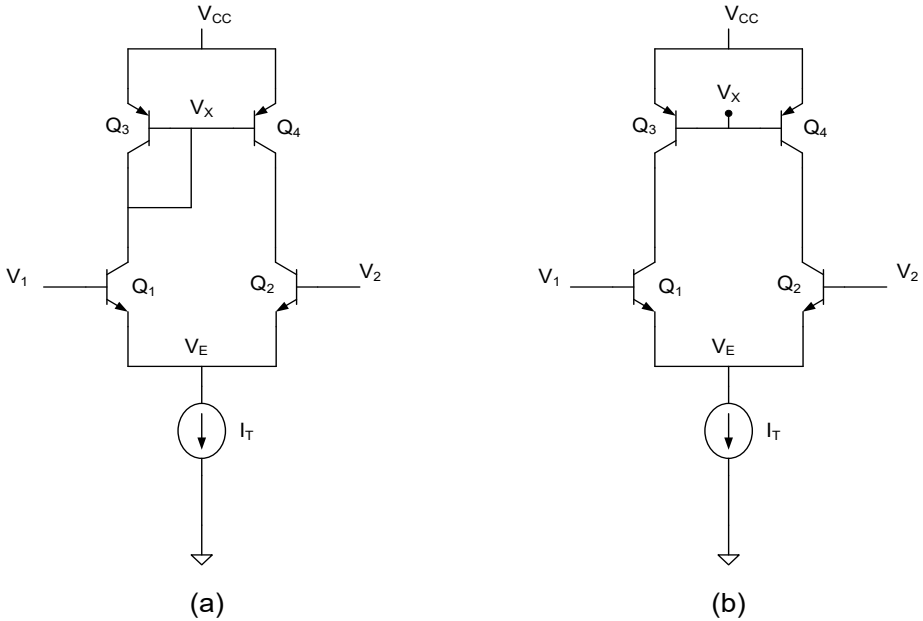
Source of Random Offset Voltages

The random offset voltage is almost entirely that of the input stage in most op amps



Review from last lecture

Random Offset Voltages



It can be shown that

$$\sigma^2_{V_{OS}} \simeq 2V_t^2\left[\frac{A^2_{Jn}}{A_{En}} + \frac{A^2_{Jp}}{A_{Ep}}\right]$$

where very approximately

$$A_{Jn} = A_{Jp} = 0.1\mu$$

Review from last lecture

Random Offset Voltages

Typical offset voltages:

MOS - 5mV to 50MV
BJT - 0.5mV to 5mV

These can be scaled with extreme device dimensions

Often more practical to include offset-compensation circuitry

Gradient Effects and Common Centroid Layouts

Random Offset Voltage

- Due to random variations in process parameters and device dimensions
- Random offset is actually a random variable at the design level but deterministic after fabrication in any specific device
- Distribution naturally nearly Gaussian (could be un-naturally manipulated)

  Has zero mean

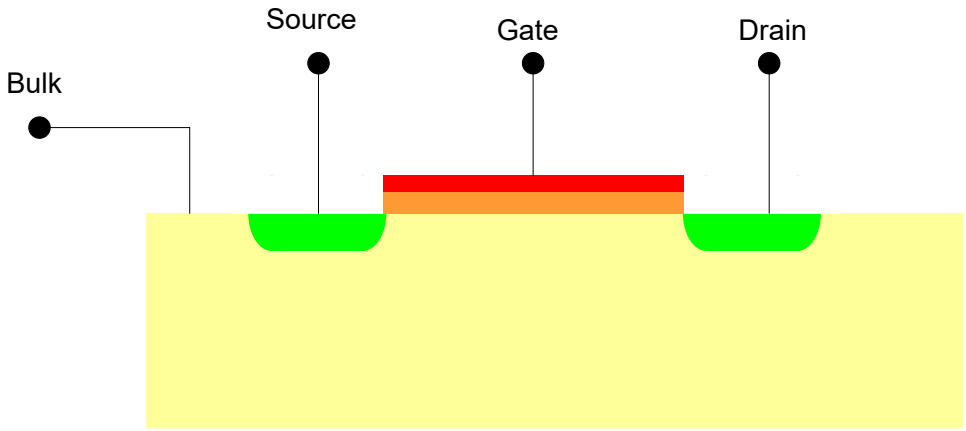
  Characterized by its standard deviation or variance

  Often strongly layout dependent

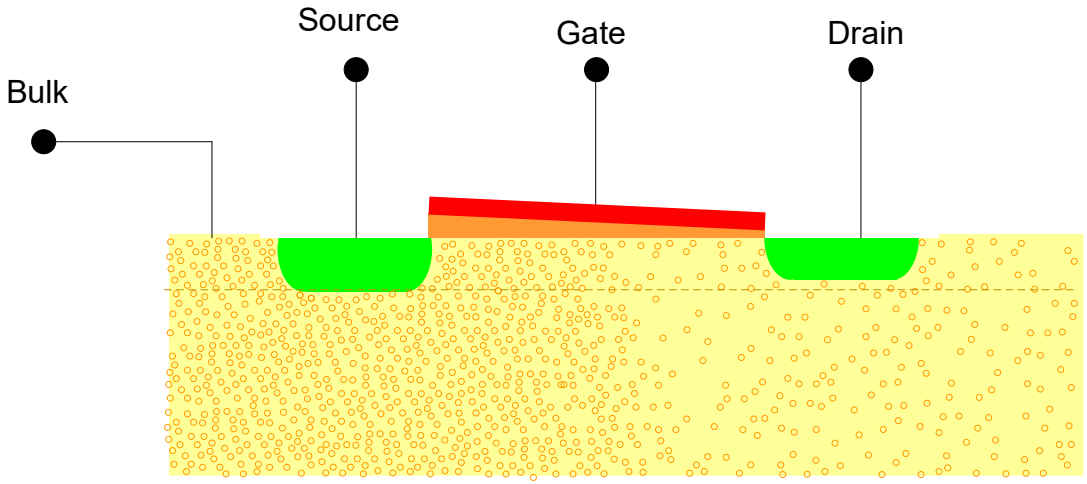
  Due to both local random variations and correlated gradient effects

  - Will consider both effects separately
  - Gradient effects usually dominate if not managed
  - Good methods exist for driving gradient effects to small levels

Offset Voltages due to Gradients



n-channel MOSFET



n-channel MOSFET

Impurity density or layer thicknesses vary linearly through the channel

Model and design parameters vary throughout channel and thus the corresponding equivalent lumped model parameters will vary from device to device

Model Parameter Variation

Define p to be a process parameter that varies with lateral position throughout the region defined by the channel of the transistor.

Almost Theorem:

If p(x,y) varies throughout a two-dimensional region, then

$$p_{EQ} = \frac{1}{A}\int_A p(x,y)\,dx\,dy$$

Parameters such at V_T, μ and C_{OX} vary throughout a two-dimensional region

Gradients

~~Local random variations~~ introduce a random component in device model parameters which are ~~uncorrelated~~ correlated for neighborhood devices but for ideally matched devices they are identically distributed e.g. $V_{TEQi}=V_{TN}+V_{TR\,i}$

V_{TRi} and V_{TRj} due to ~~local random variations~~ gradients are ~~uncorrelated~~ correlated for i≠j but if ideally matched they are identically distributed

Common Centroid Layouts

Define p to be a process parameter that varies linearly with lateral position throughout the region defined by the channel of the transistor.

Almost Theorem:

If p(x,y) varies linearly throughout a two-dimensional region, then

$$p_{EQ} = \frac{1}{A}\int_A p(x,y)\,dx\,dy$$

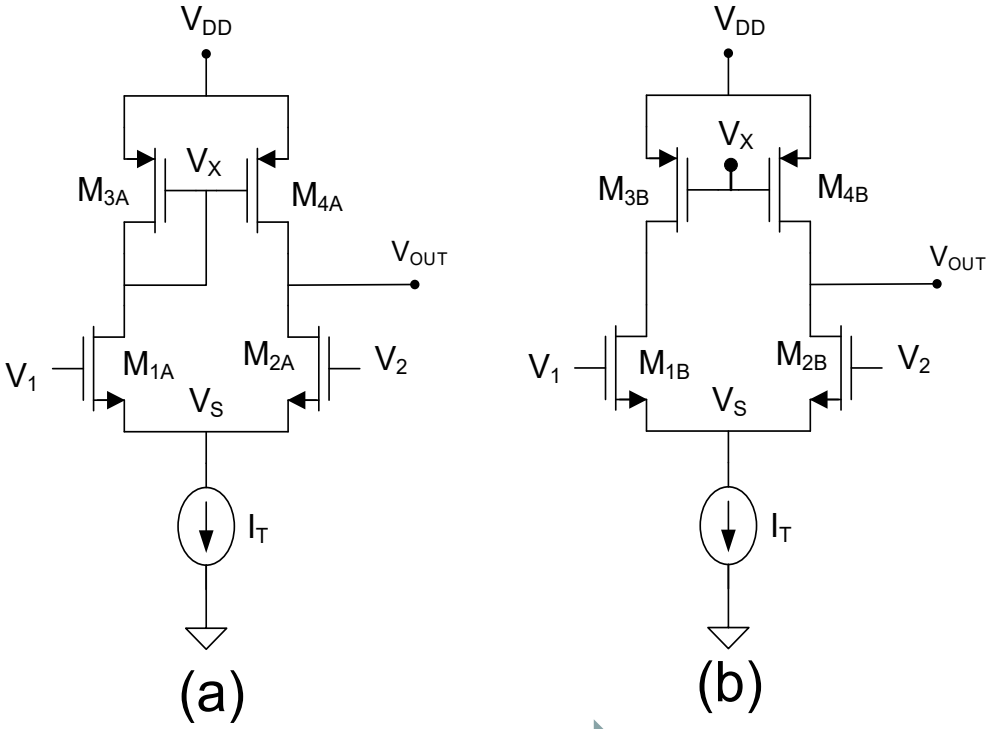
Gradient effects cause parameters such at V_T, μ and C_{OX} to vary approximately linearly throughout a two-dimensional region

The direction and magnitude of gradients are random variables but are correlated and identical for closely-placed devices

Source of Random Offset Voltages

The random offset voltage is almost entirely that of the input stage in most op amps

Assume schematic representative of placement of devices in layout



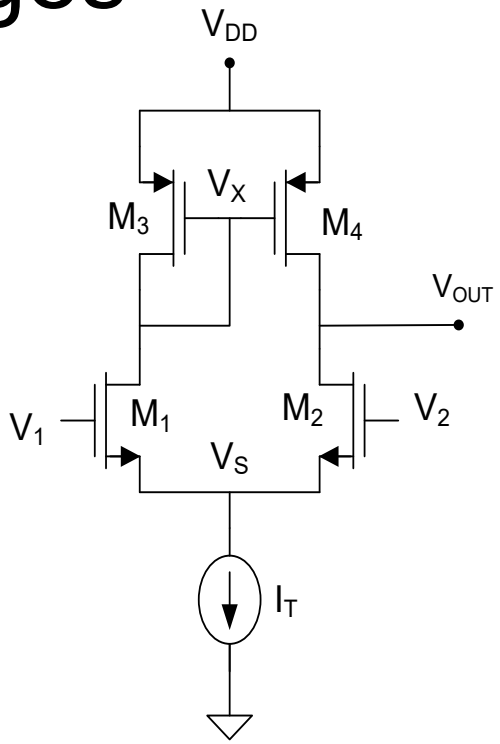
If threshold gradient in this direction and local random variations are neglected

$$V_{TH2A} = V_{TH1A} + \alpha d$$

α is the magnitude of the gradient

d is the distance between M_{1A} and M_{2A}

Random Offset Voltages



The random offset associated with local random variations is due to missmatches in the four transistors, dominantly missmatches in the parameters {V_T, μ,C_{OX},W and L}

Gradient effects and local random variations are both present and additive

$$V_{Ti}=V_{TN}+V_{TRi}+V_{TGi}$$

$$C_{OXi}=C_{OXN}+C_{OXRi}+C_{OXGi}$$

$$\mu_i=\mu_N+\mu_{Ri}+\mu_{Gi}$$

$$W_i=W_N+W_{ri}+W_{Gi}$$

$$L_i=L_N+L_{ri}+L_{Gi}$$

Each design and model parameter is comprised of a nominal part and a random component

The local random parts of each model parameter are uncorrelated but if ideally matched are identically distributed and the gradient parts for closely placed devices are correlated

Gradients are uncorrelated with local random variations

Recall:

Model Parameter Variations

Define p to be a process parameter that varies with lateral position throughout the region defined by the channel of the transistor.

Almost Theorem:

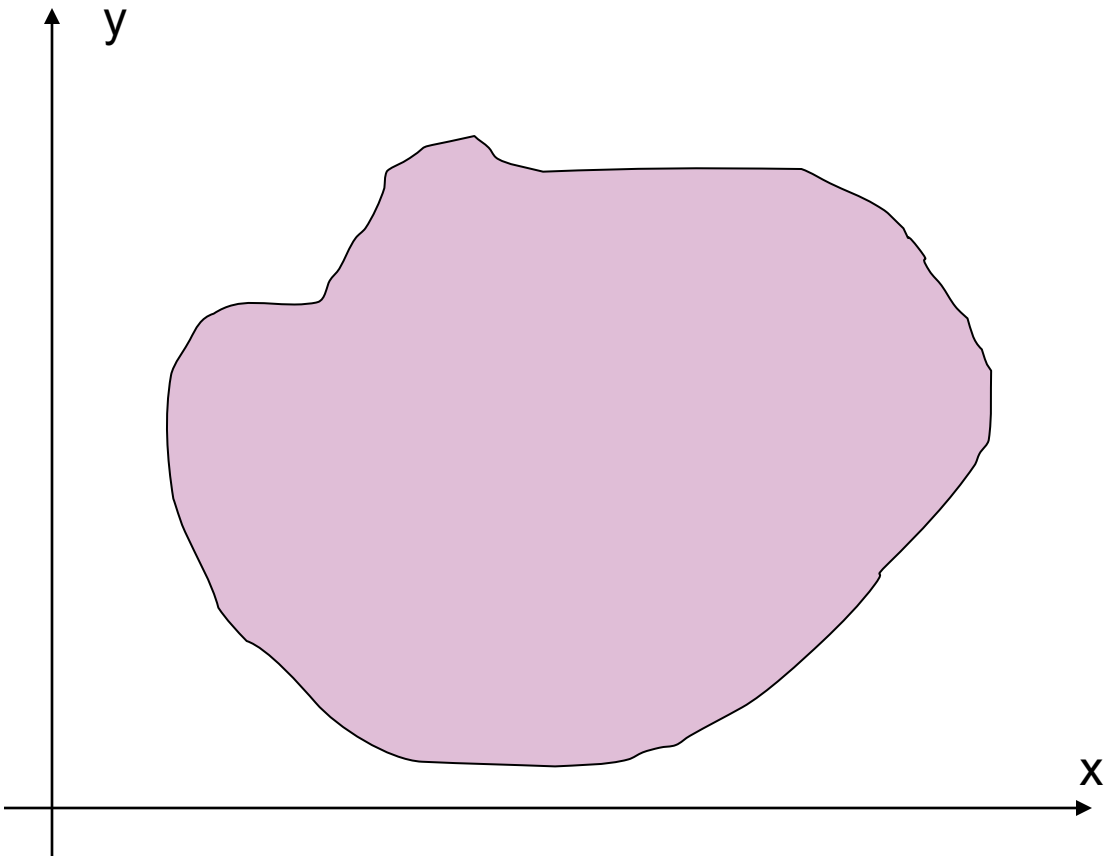
If p(x,y) varies throughout a two-dimensional region, then

$$p_{EQ} = \frac{1}{A}\int_{A} p(x,y)\,dx\,dy$$

Parameters such at V_T, μ and C_{OX} vary throughout a two-dimensional region

Recall:

Model Parameter Variations



$$p_{EQ} = \frac{1}{A}\int_{A} p(x,y)\,dx\,dy$$

Common Centroid Layouts

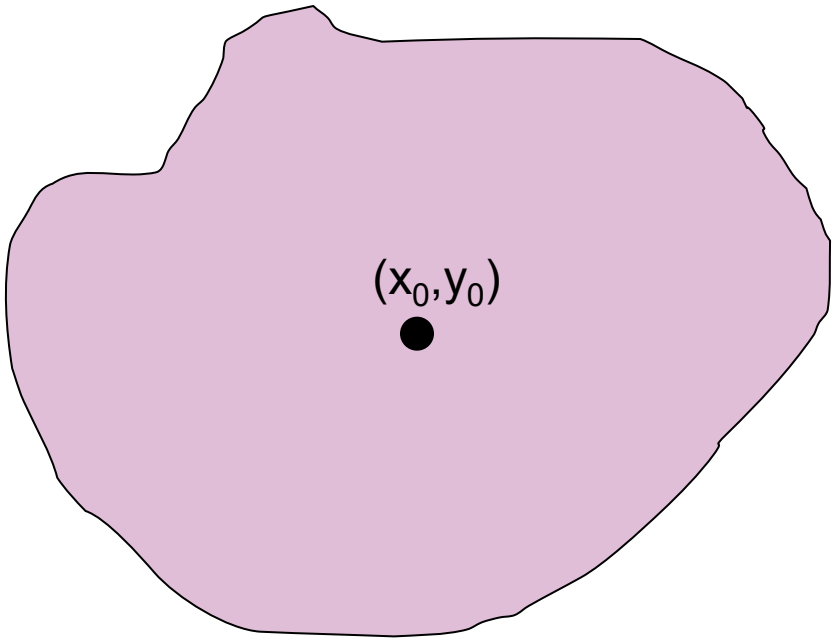
Almost Theorem:

If p(x,y) varies linearly throughout a two-dimensional region, then $p_{EQ}=p(x_0.y_0)$ where x_0,y_0 is the geometric centroid to the region.

If a parameter varies linearly throughout a two-dimensional region, it is said to have a linear gradient.

Many parameters have a dominantly linear gradient over rather small regions but large enough to encompass layouts where devices are ideally matched

Common Centroid Layouts



(x_0,y_0) is geometric centroid

$$p_{EQ} = \frac{1}{A}\int_A p(x,y)\,dx\,dy$$

If ρ(x,y) varies linearly in any direction, then the theorem states

$$p_{EQ} = \frac{1}{A}\int_A p(x,y)\,dx\,dy = p(x_0,y_0)$$

Common Centroid Layouts

Definition: A layout of two devices is termed a common-centroid layout if both devices have the same geometric centroid

Almost Theorem:

If p(x,y) varies linearly throughout a two-dimensional region, then if two devices have the same centroid, the linear-variable parameters are matched !

Note: This is true independent of the magnitude and direction of the gradient!

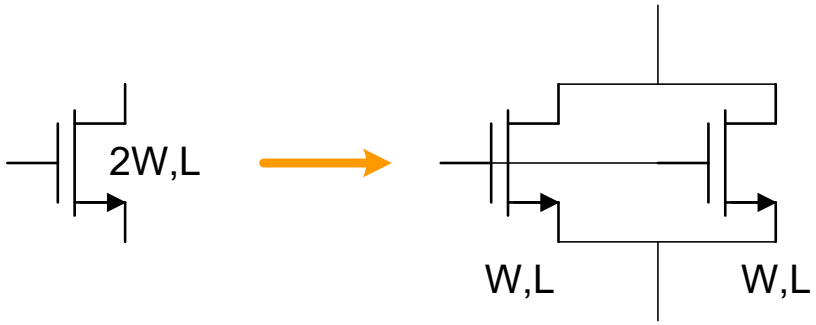
Almost Theorem:

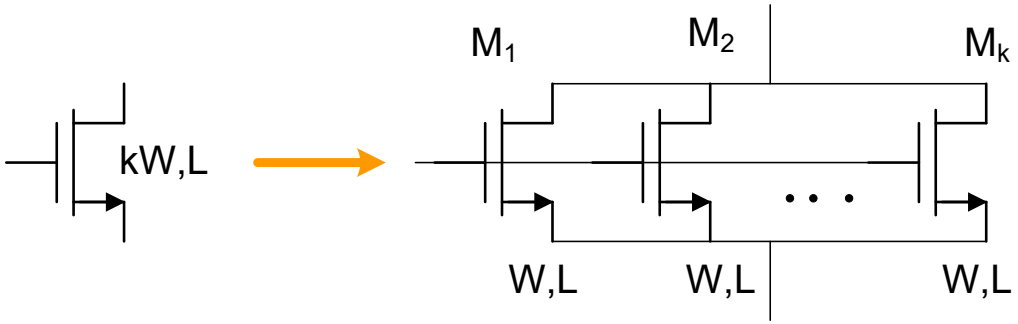
If a common-centroid layout is used for the matching-critical part of an operational amplifier, the linear part of the linear-variable parameters (e.g. V_{TH}, μ, C_{OX}) will introduce no offset voltage!

Common-centroid layouts almost always used for matching-critical components to eliminate linear gradients of critical parameters !

But local random variations will still affect matching even if gradient effects are eliminated

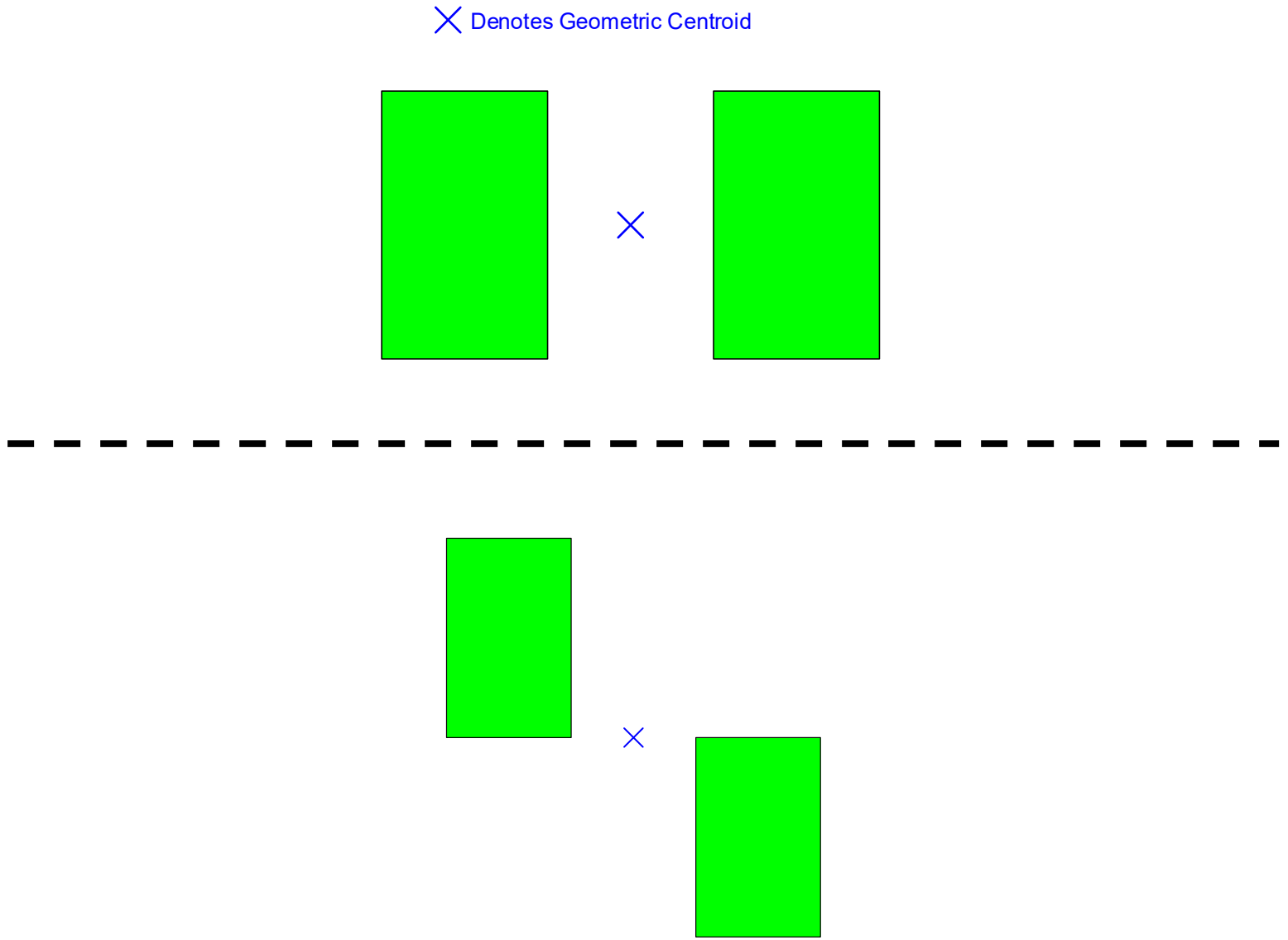
Recall parallel combinations of transistors equivalent to a single transistor of appropriate W,L



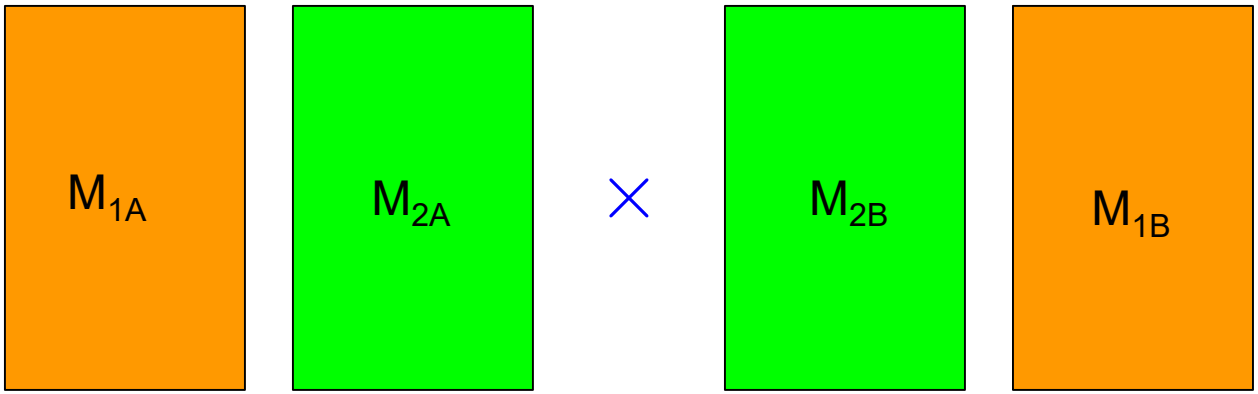


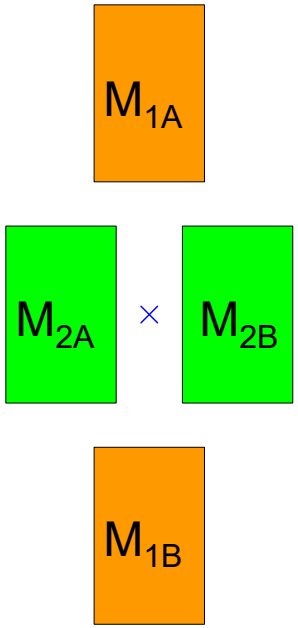
A single device is comprised of a parallel interconnection of smaller devices is termed a segmented structure

Centroids of Segmented Geometries



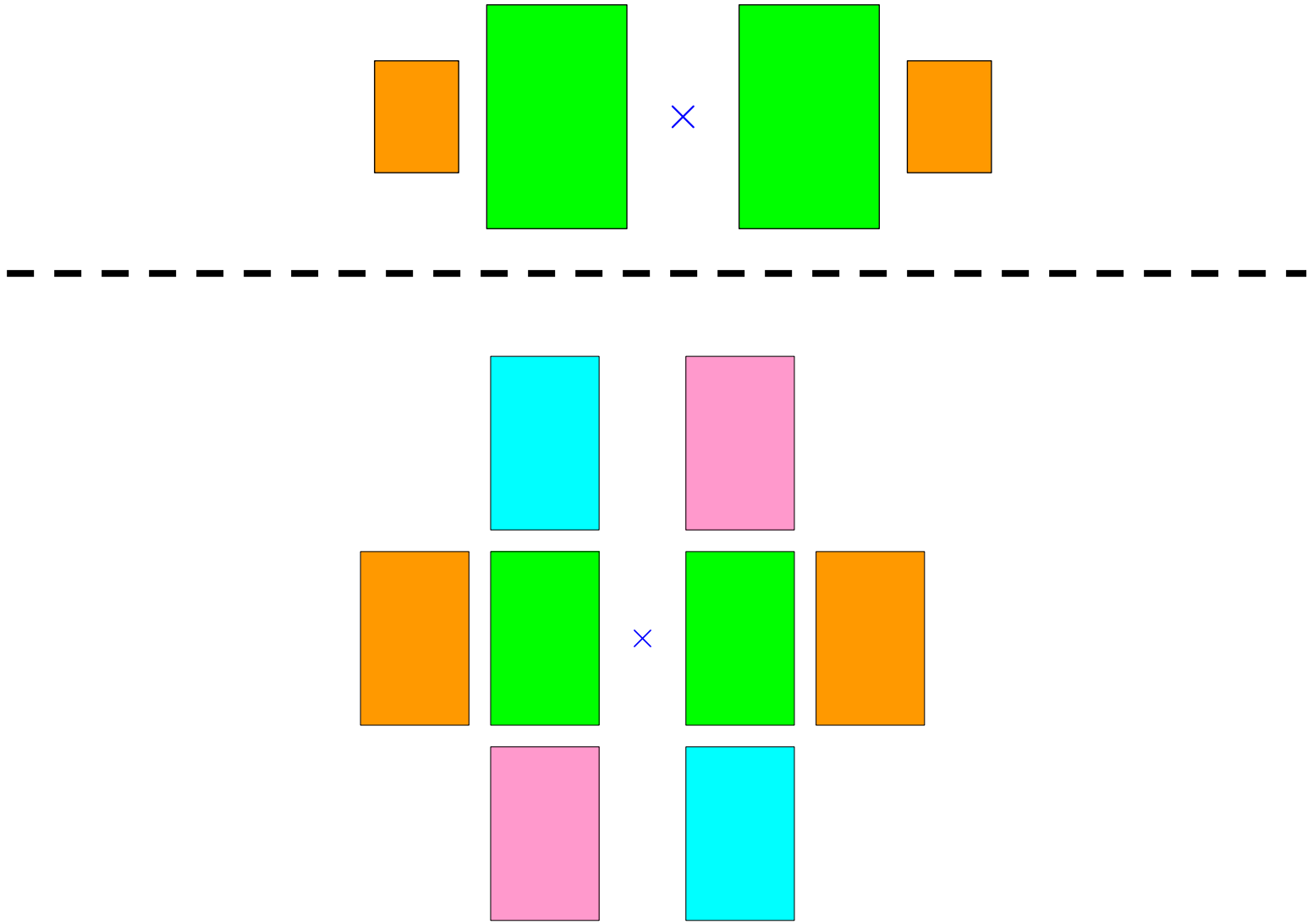
Common Centroid of Multiple Segmented Geometries



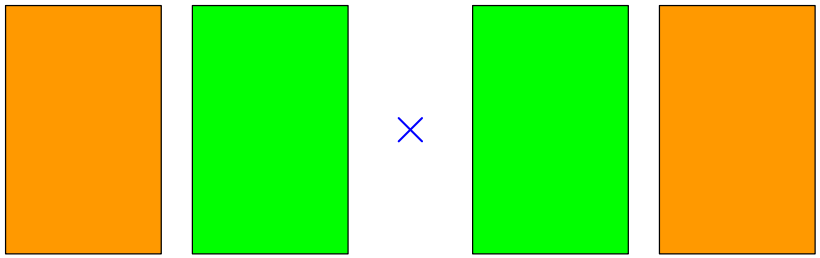


If these are layouts of gates of two transistors with two segments, M_1 and M_2 have common centroids. They are thus termed common-centroid layouts

Common Centroid of Multiple Segmented Geometries



Common Centroid Layouts



Common centroid layouts widely (almost always) used where matching of devices or components is critical because these layouts will cancel all first-order gradient effects

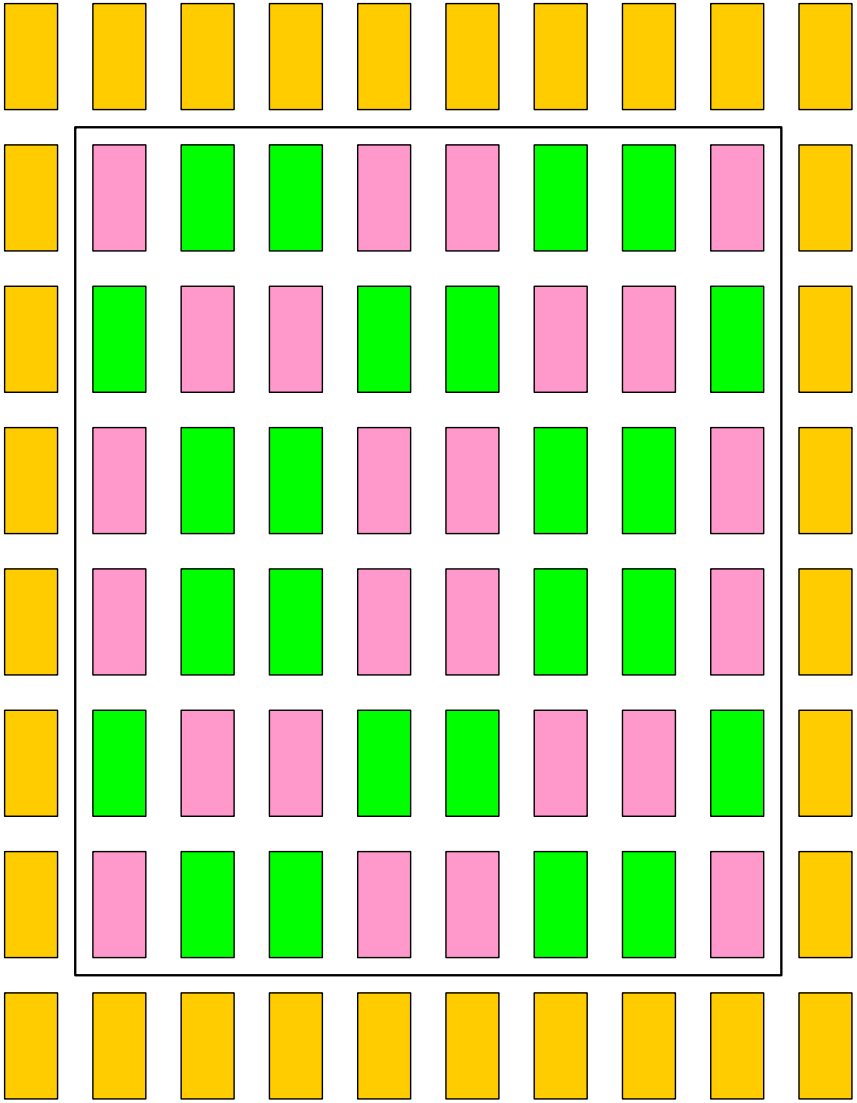
Applies to resistors, capacitors, transistors and other components

Always orient all devices in the same way

Keep common centroid for interconnects, diffusions, and all features

Often dummy devices placed on periphery to improve matching !

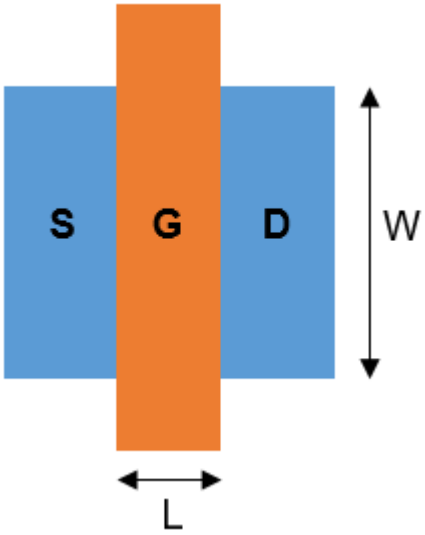
Common Centroid Layout Surrounded by Dummy Devices



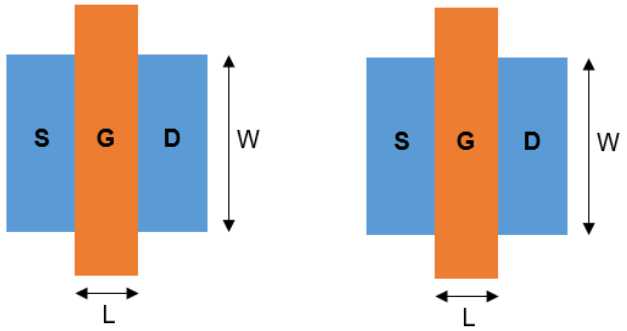
Fingers and Multipliers

- Multiple fingers use shared diffusions
- Multipliers refer to multiple copies of transistors with individual drains and sources

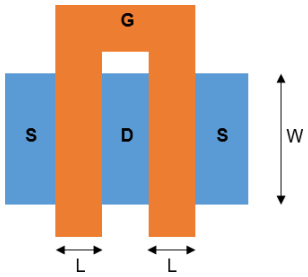
Important to match orientation if overall device matching is required



Multiplier = 2

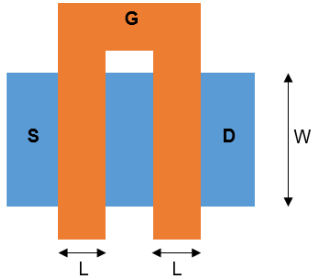


Fingers = 2



$L_{eff}=L$, $W_{eff}=2W$

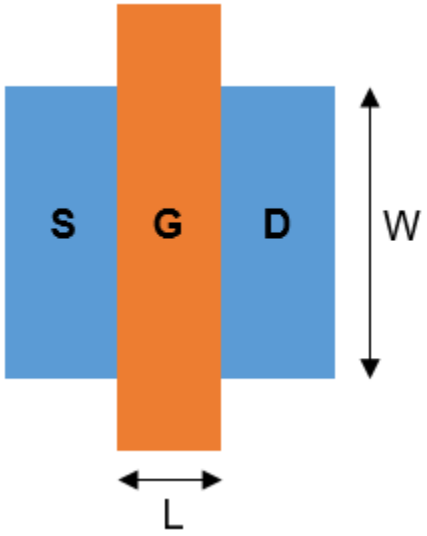
Fingers = 2



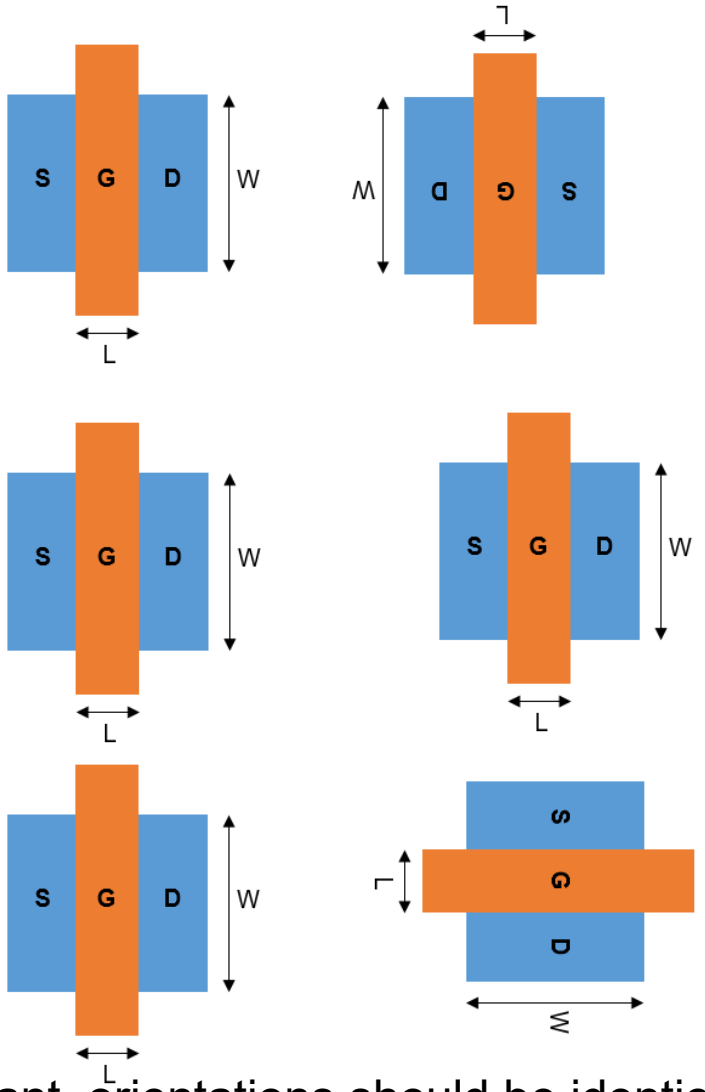
$L_{eff}=2L$, $W_{eff}=W$

https://electronics.stackexchange.com/questions/246463/multiple-fingers-vs-single-finger-layout-mosfet-transistor

Fingers and Multipliers



Alternate Orientations



If matching is important, orientations should be identical

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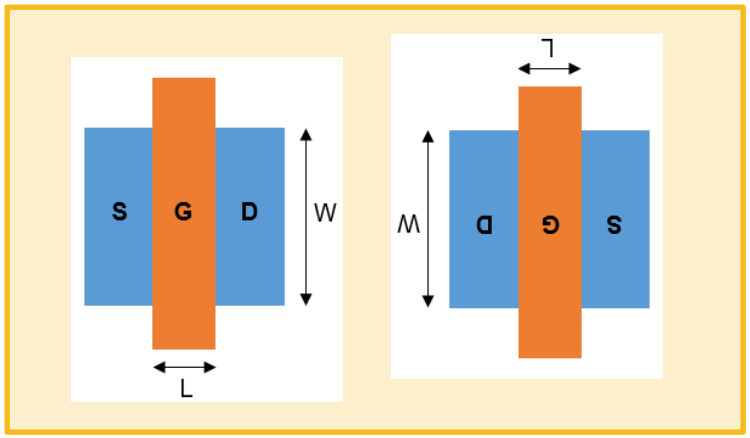
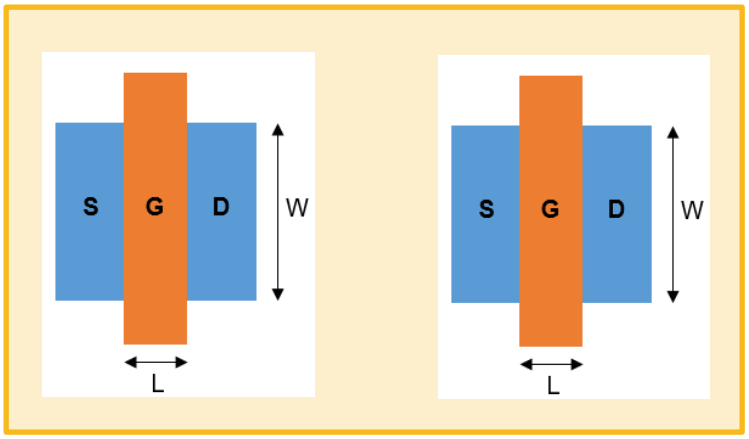
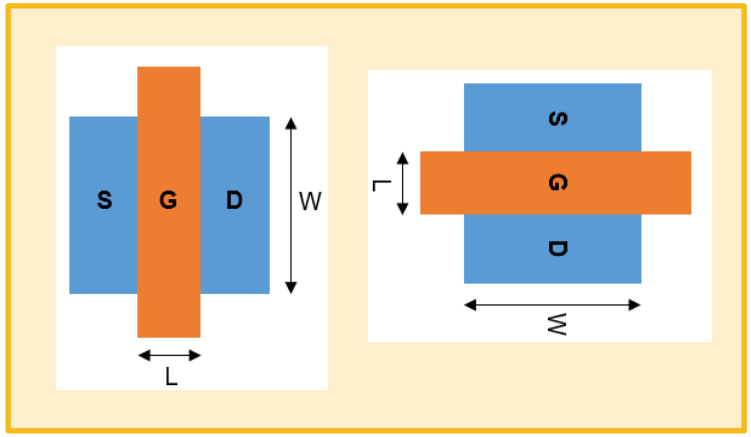
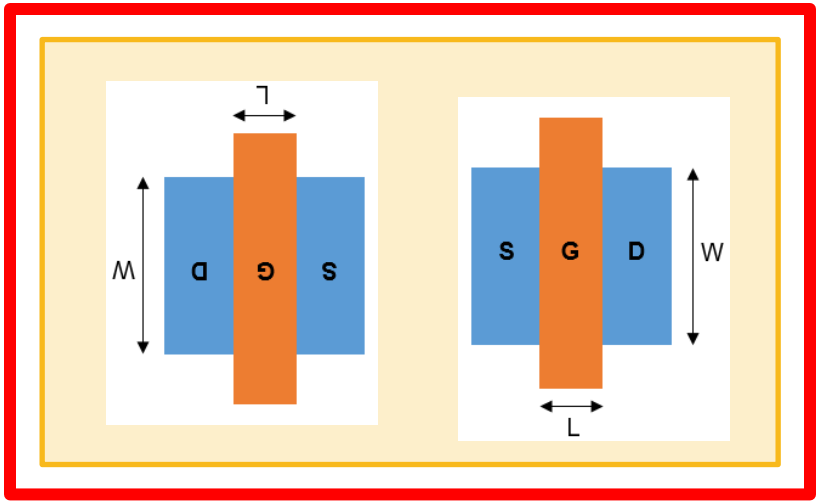
Fingers and Multipliers

Alternate Orientations







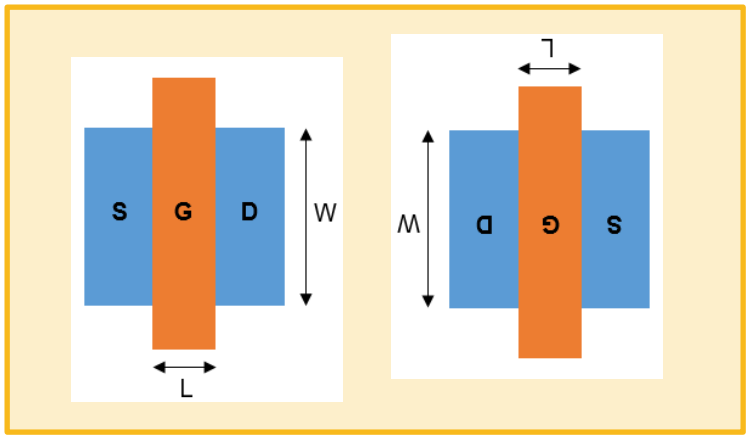


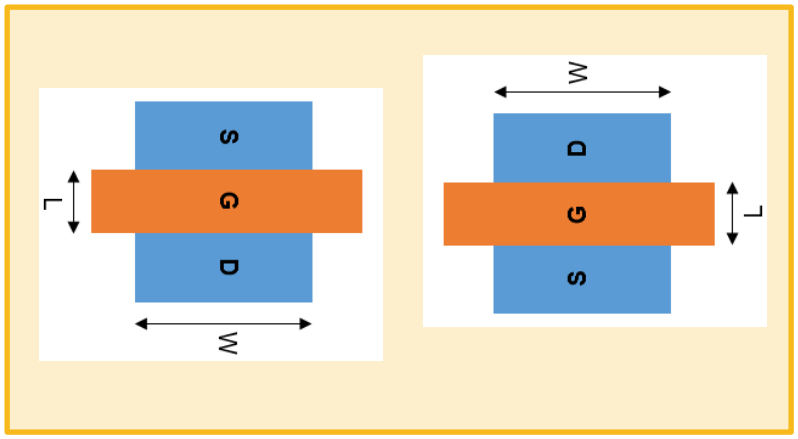
Which layout would be best for the critical differential input pair in an operational amplifier?

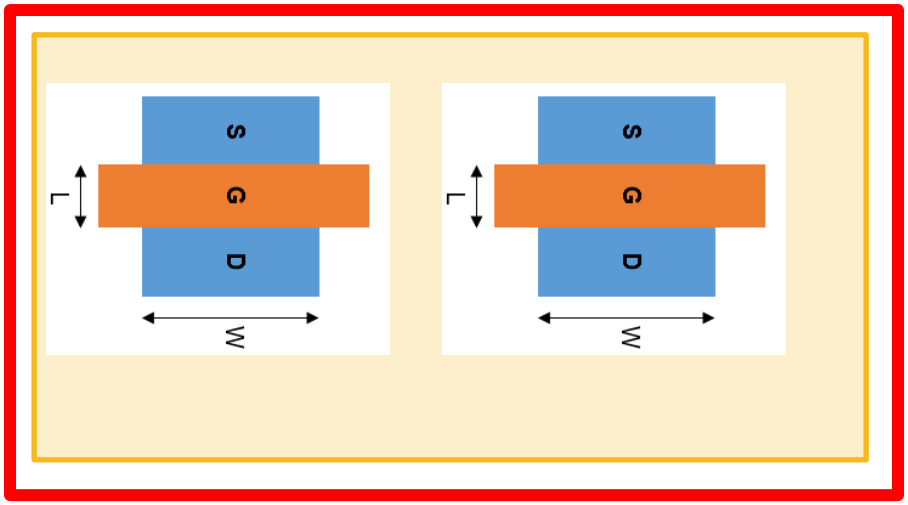
Of course, a common-centroid variant would likely be used !

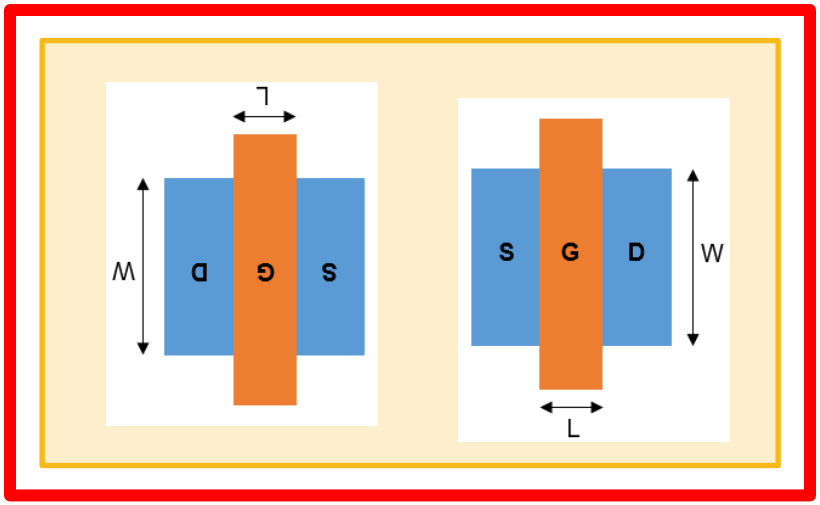
Fingers and Multipliers

Alternate Orientations





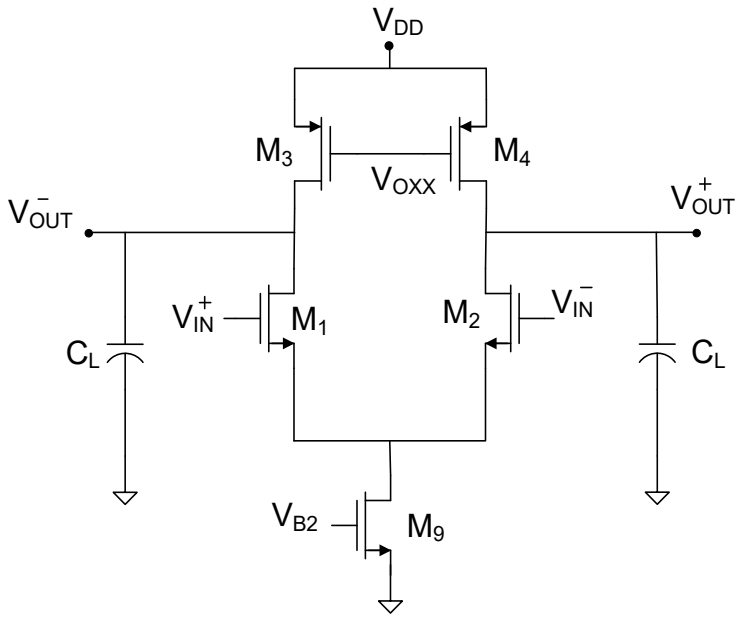




Which layout would be best for the critical differential input pair in an operational amplifier?

Of course, a common-centroid variant would likely be used !

Common-Mode Feedback

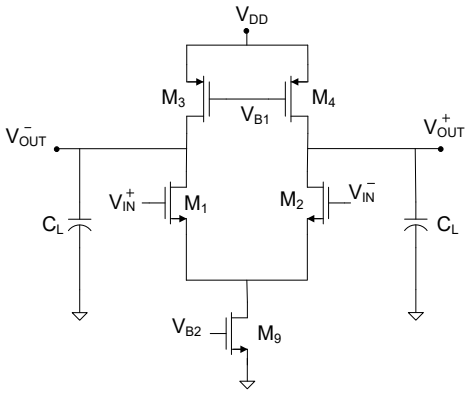


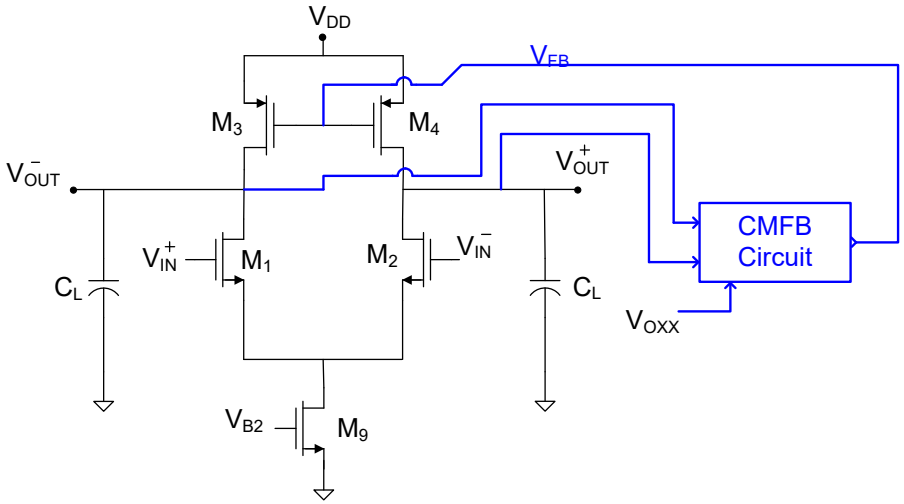
Needs CMFB

Repeatedly throughout the course, we have added a footnote on fully-differential circuits that a common-mode feedback circuit (CMFB) is needed for some circuits

If required, the CMFB circuit establishes or “stabilizes” the operating point or operating points of the op amp

Common-Mode Feedback





On the reference op amp, the CMFB signal can be applied to either the p-channel biasing transistors or to the tail current transistor

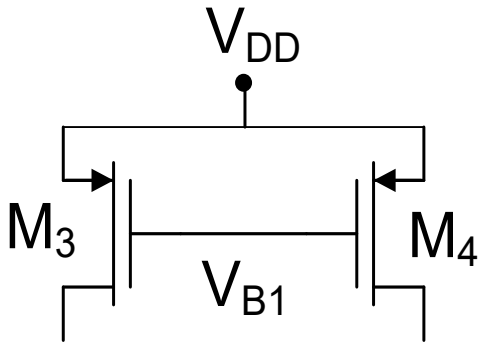
It is usually applied only to a small portion of the biasing transistors though often depicted as shown

There is often considerable effort devoted to the design of the CMFB though little details are provided in most books and the basic concepts of the CMFB are seldom rigorously developed and often misunderstood

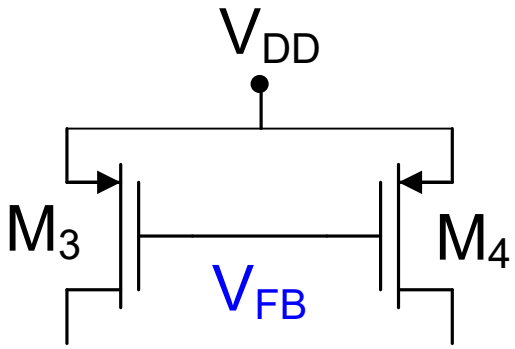
Common-Mode Feedback

Partitioning biasing transistors for V_{FB} insertion

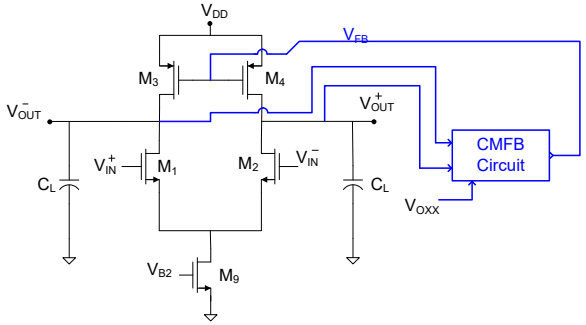
(Nominal device matching assumed, all L's equal)

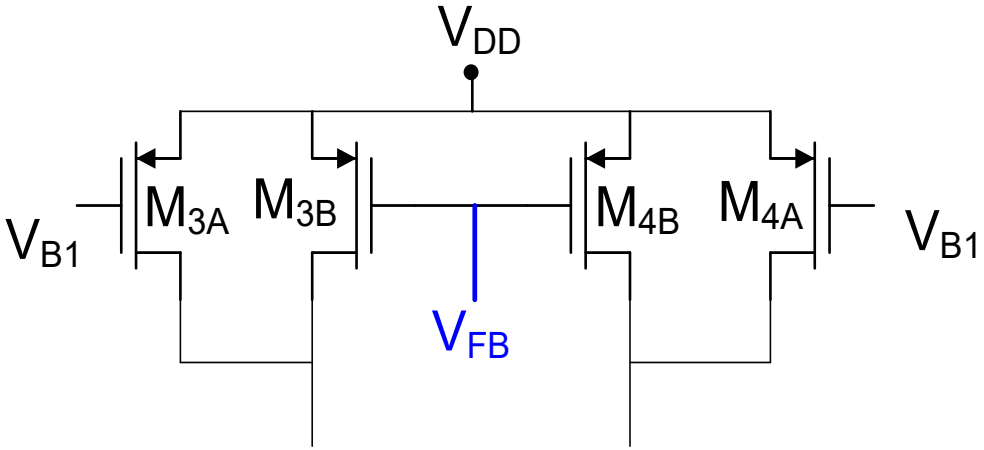


Ideal (Desired) biasing



V_{FB} insertion





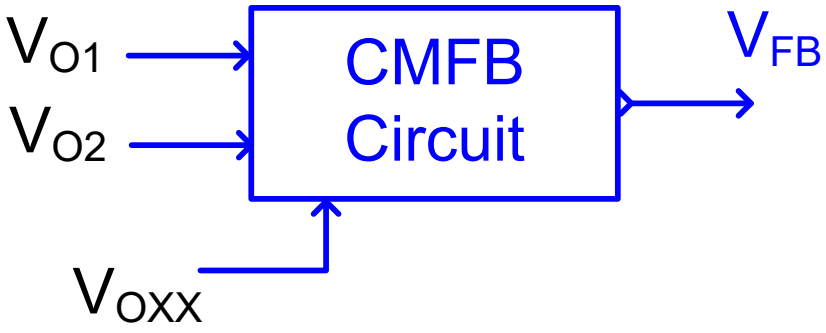
Partitioned V_{FB} insertion

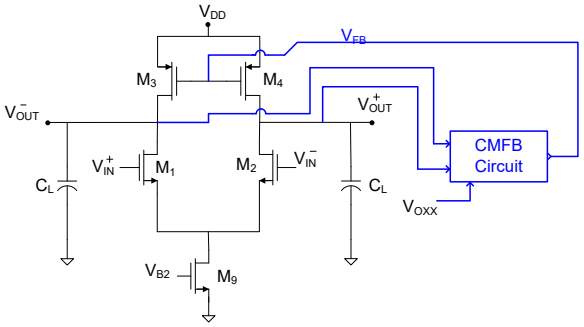
$$W_{3A} + W_{3B} = W_3$$

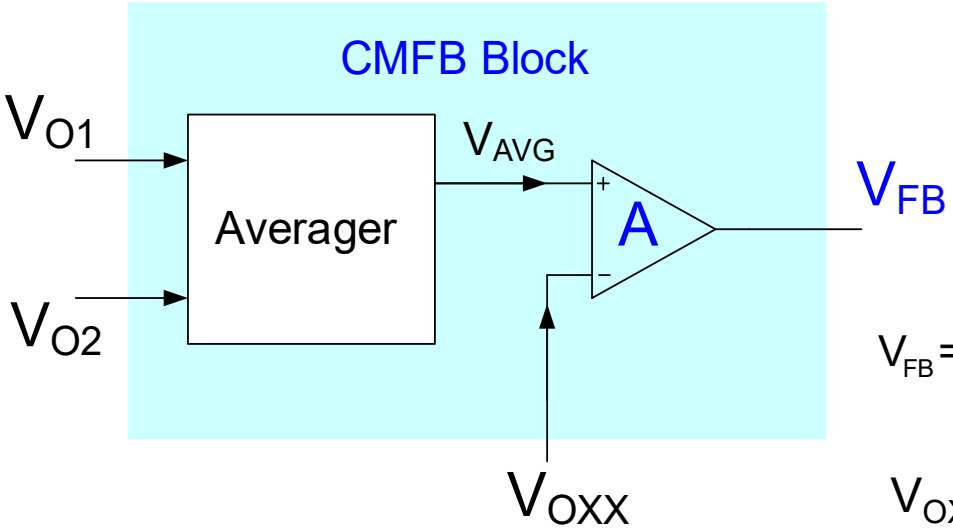
$$W_{3B} << W_{3A}$$

Of course L/R symmetry is assumed

Basic Operation of CMFB Block



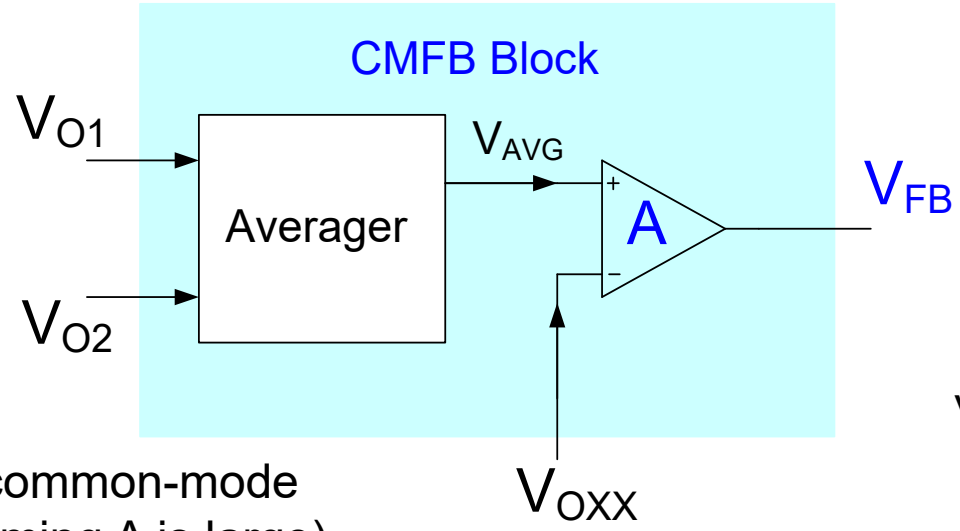




$$V_{FB} = \left(\frac{V_{01} + V_{02}}{2} \right) A(s)$$

V_{OXX} is the desired quiescent voltage at the stabilization node
(irrespective of where V_{FB} goes)

Basic Operation of CMFB Block



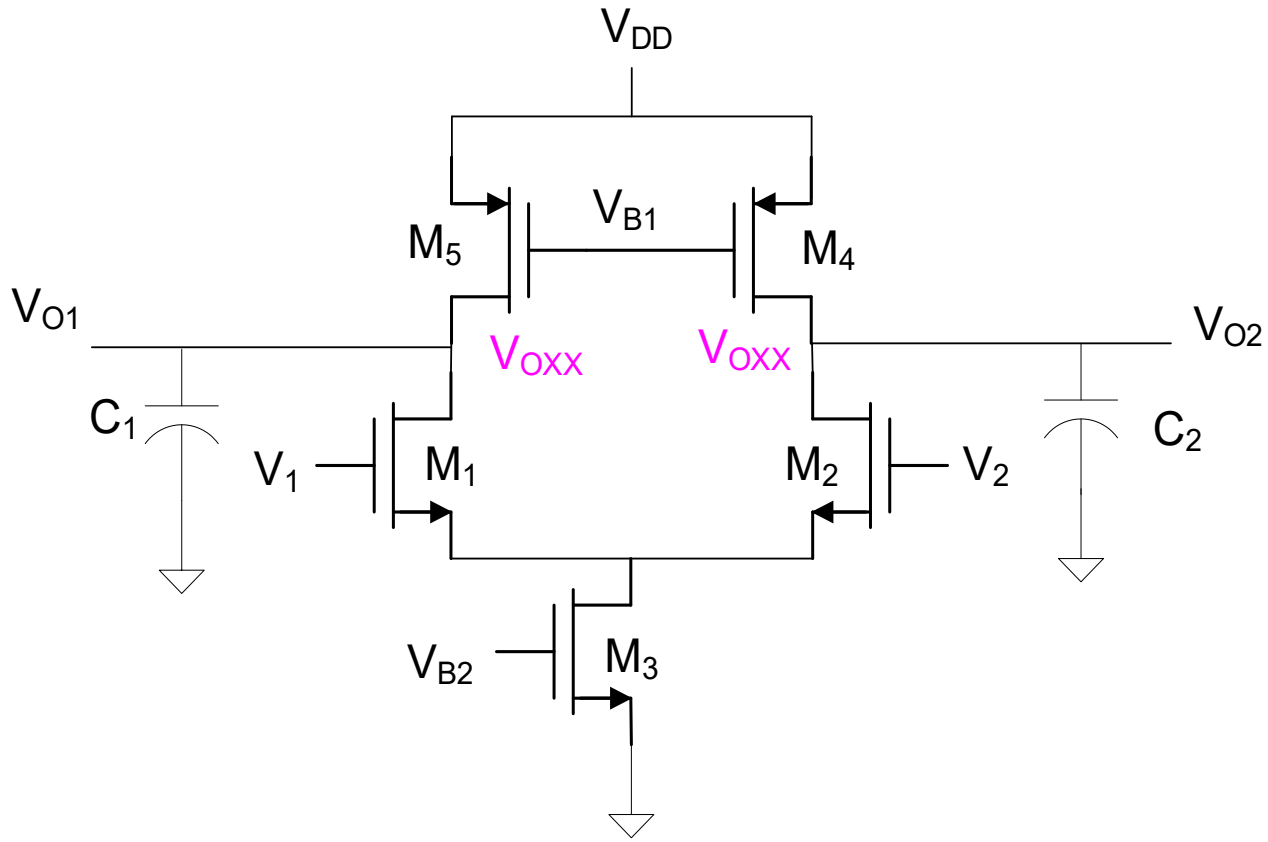
$$V_{FB}=\left(\frac{V_{01}+V_{02}}{2}\right)A(s)$$

V_{OXX} is the desired common-mode output voltage (assuming A is large)

- Comprised of two fundamental blocks
  - Averager
  - Differential amplifier
- Sometimes combined into single circuit block
- CMFB is often a two-stage amplifier so compensation of the CMFB path often required !!

Mathematics behind CMFB

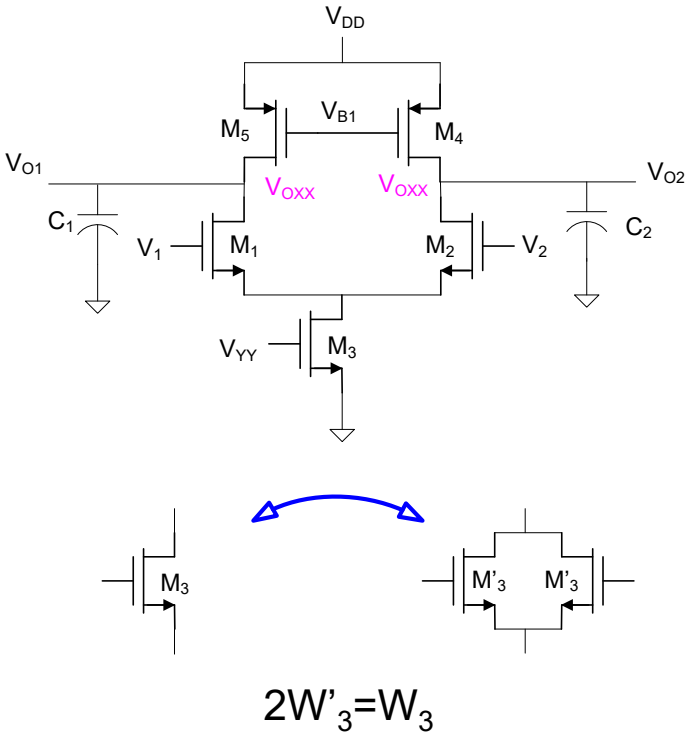
(consider an example that needs a CMFB)

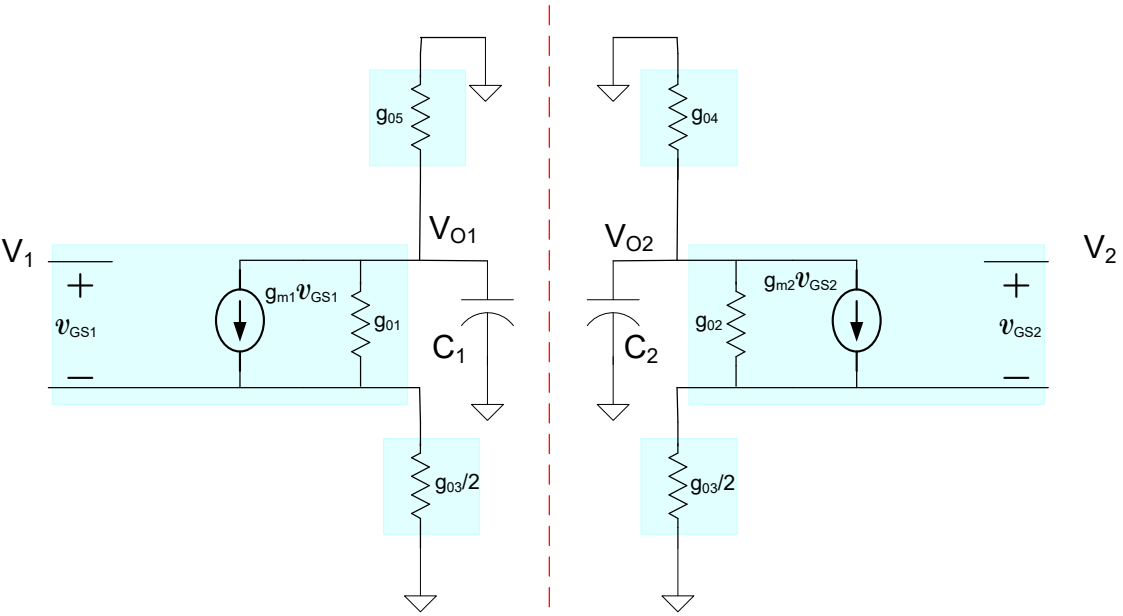


Notice there are two capacitors and thus two poles in this circuit

Mathematics behind CMFB

(consider an example that needs a CMFB)



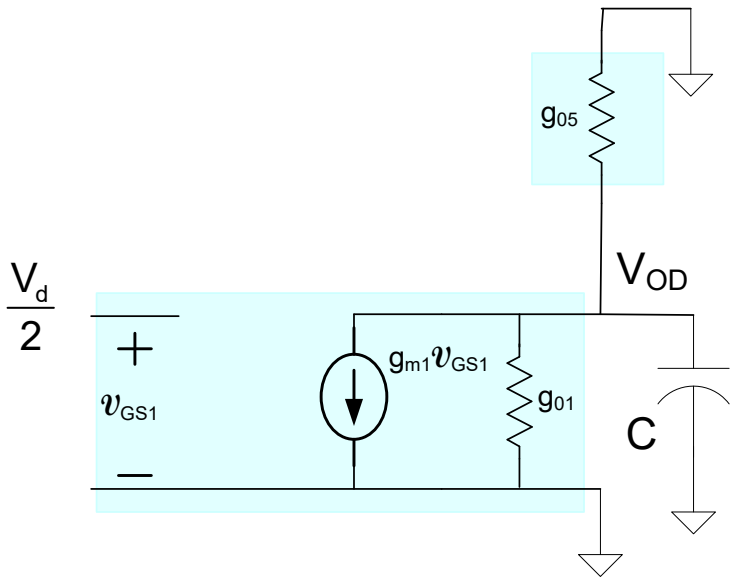


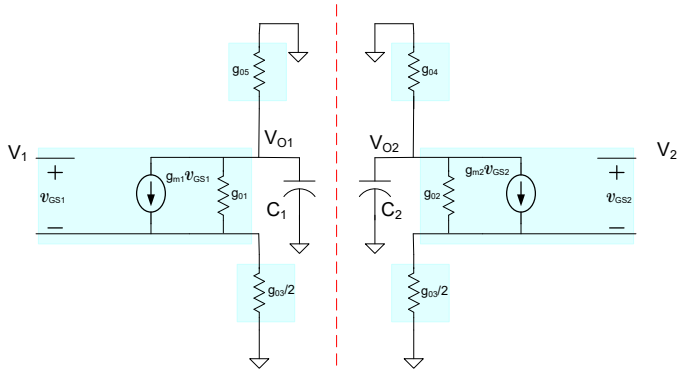
Small-signal model showing axis of symmetry (for $V_1=V_2=V_{INQ}$ i.e. $v_1=v_2=0V$)

What order transfer functions are expected (note two capacitors!)?

Mathematics behind CMFB

(consider an example that needs a CMFB)





Small-signal difference-mode half circuit

$$V_{OD}\left(sC+g_{01}+g_{05}\right)+g_{m1}\frac{V_d}{2}=0$$

$$A_{DIFF}=\frac{-\frac{g_{m1}}{2}}{sC+g_{01}+g_{05}}$$

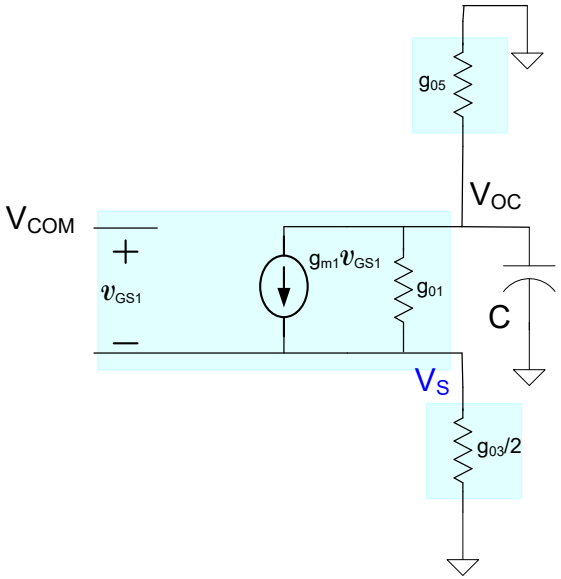
$$p_{DIFF}=-\frac{g_{01}+g_{05}}{C}$$

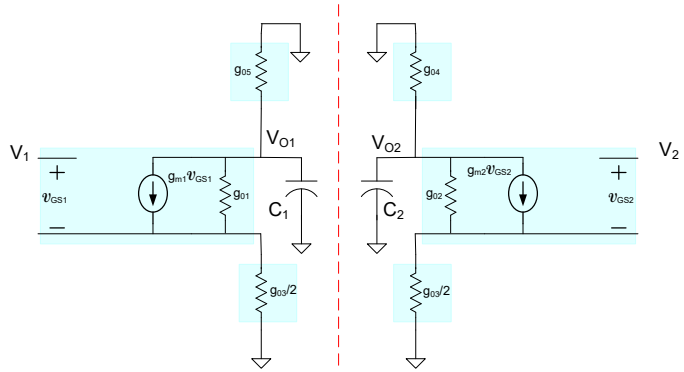
Note there is a single-pole in this circuit

What happened to the other pole?

Mathematics behind CMFB

(consider an example that needs a CMFB)





Standard small-signal common-mode half circuit

$$V_{OC}(sC+g_{01}+g_{05})+g_{m1}(V_{COM}-V_S)=0$$

$$V_S(g_{01}+g_{03}/2)-g_{m1}(V_{COM}-V_S)=V_{OC}g_{01}$$

$$A_{COM}=\frac{-g_{m1}(g_{01}+g_{03}/2)}{(sC+g_{01}+g_{05})(g_{m1}+g_{01}+g_{03}/2)-g_{m1}g_{01}}\cong-\frac{g_{01}+g_{03}/2}{sC+g_{05}}$$

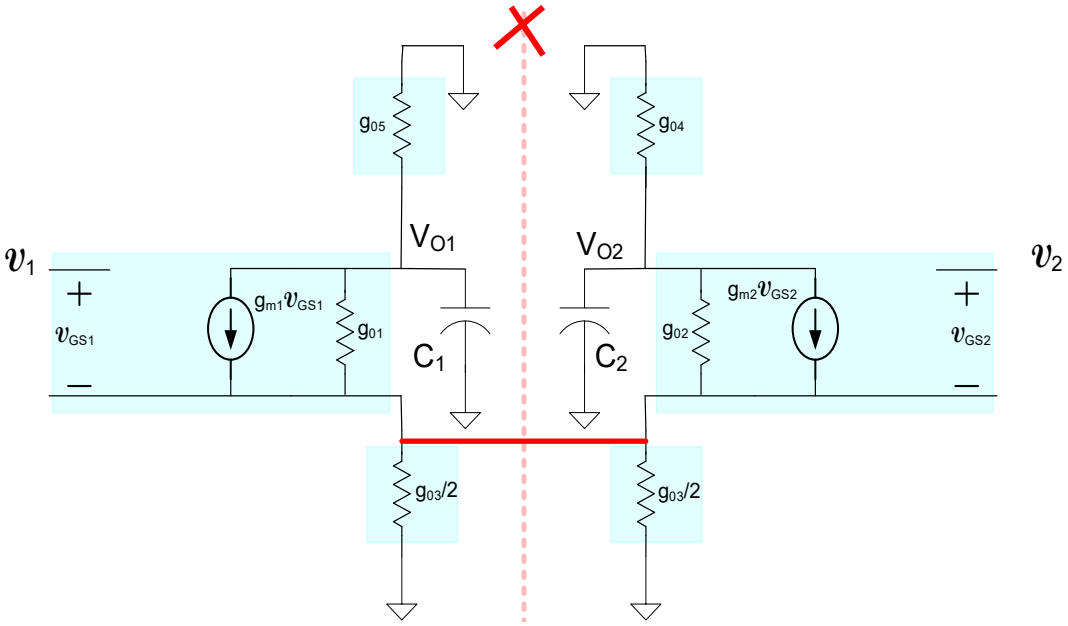
$$p_{COM}=-\frac{g_{05}}{C}$$

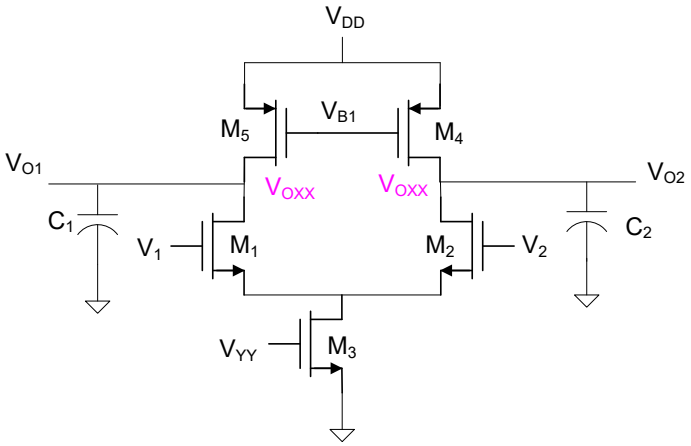
Note there is a single-pole in this circuit

And this is different from the difference-mode pole

But the common-mode gain tells little, if anything, about the CMFB

Mathematics behind CMFB





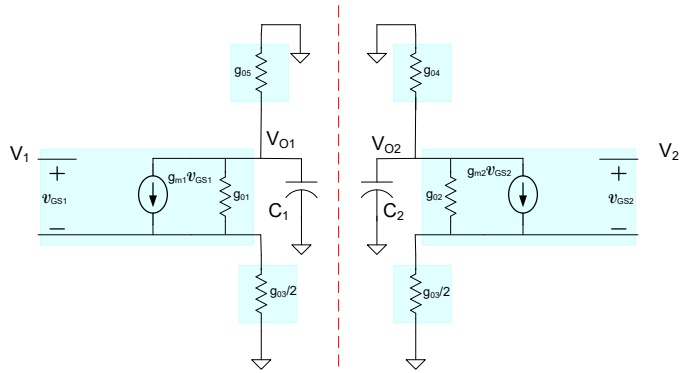
Second-order gain functions would have occurred had we not created symmetric half-circuits by assuming v_1=v_2

Mathematics behind CMFB

(consider an example that needs a CMFB)

$$A_{COM} \simeq -\frac{g_{01}+g_{03}/2}{sC+g_{05}} \qquad p_{COM} = -\frac{g_{05}}{C}$$

$$A_{DIFF} = \frac{-\frac{g_{m1}}{2}}{sC+g_{01}+g_{05}} \qquad p_{DIFF} = -\frac{g_{01}+g_{05}}{C}$$



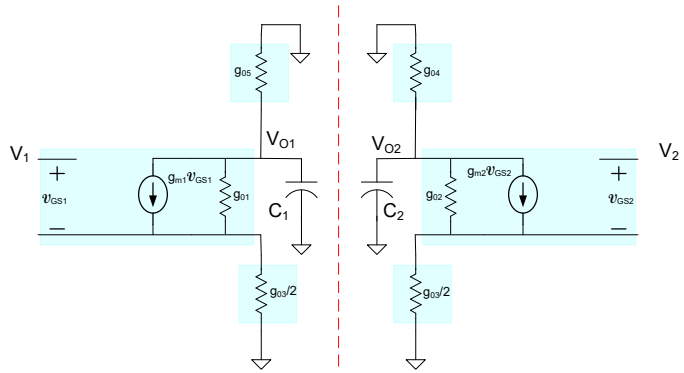
- Difference-mode analysis of symmetric circuit completely hides all information about common-mode
- This also happens in simulations
- Common-mode analysis of symmetric circuit completely hides all information about difference-mode
- This also happens in simulations
- Difference-mode poles may move into RHP (for two-stage structures) with FB so compensation is required for proper operation (or stabilization)
- Common-mode poles may move into RHP (for two-stage structures) with FB so compensation is required for proper operation (or stabilization)
- Difference-mode simulations tell nothing about compensation requirements for common-mode feedback
- Common-mode simulations tell nothing about compensation requirements for difference-mode feedback

Mathematics behind CMFB

(consider an example that needs a CMFB)

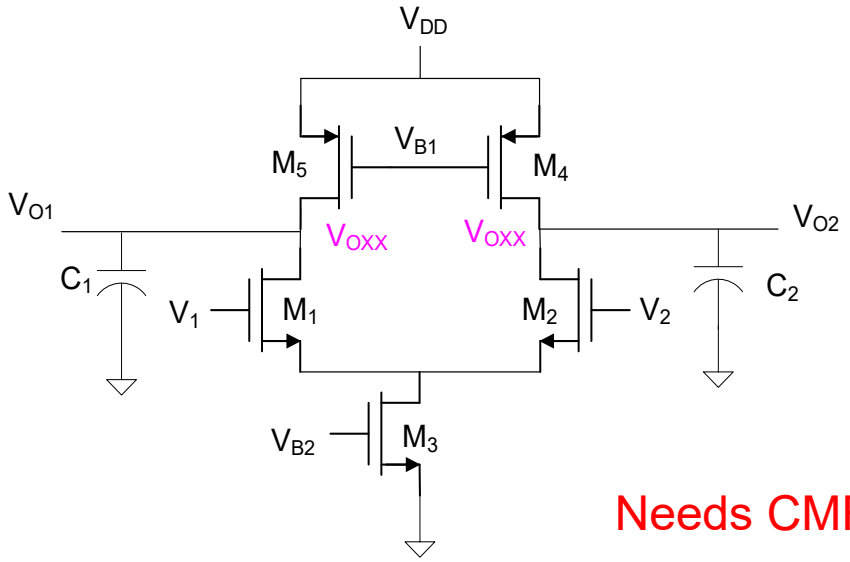
$$A_{COM} \simeq -\frac{g_{01}+g_{03}/2}{sC+g_{05}} \qquad p_{COM} = -\frac{g_{05}}{C}$$

$$A_{DIFF} = \frac{-\frac{g_{m1}}{2}}{sC+g_{01}+g_{05}} \qquad p_{DIFF} = -\frac{g_{01}+g_{05}}{C}$$



- Common-mode and difference-mode gain expressions often include same components though some may be completely absent in one or the other mode
- Compensation capacitors can be large for compensating either the common-mode or difference-mode circuits
- Highly desirable to have the same compensation capacitor serve as the compensation capacitor for both difference-mode and common-mode operation
  - But tradeoffs may need to be made in phase margin for both modes if this is done
- Better understanding of common-mode feedback is needed to provide good solutions to the problem

Does this amplifier need compensation?



Needs CMFB

No – because it is a single-stage amplifier ?

The difference-mode circuit of this 5T op amp usually does not need compensation ?

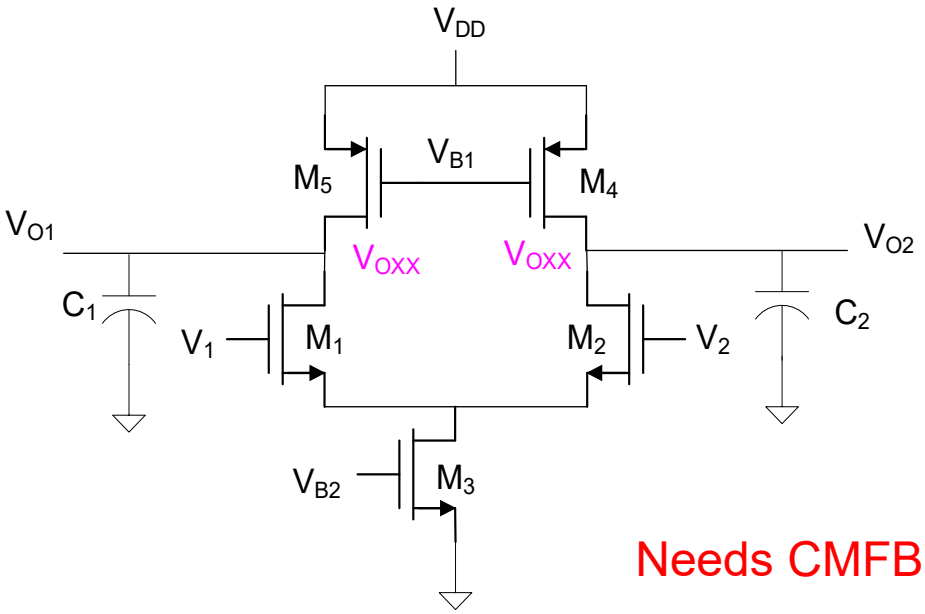
But what about the common-mode operation?

No – because the common-mode circuit is also a single-stage circuit?

What are the common-mode inputs for CMFB? **V_{B1} or V_{B2}**

But observe that the common-mode inputs V_{1C} and V_{2C} are not the common-mode inputs for the CMFB?

Does this amplifier need compensation?



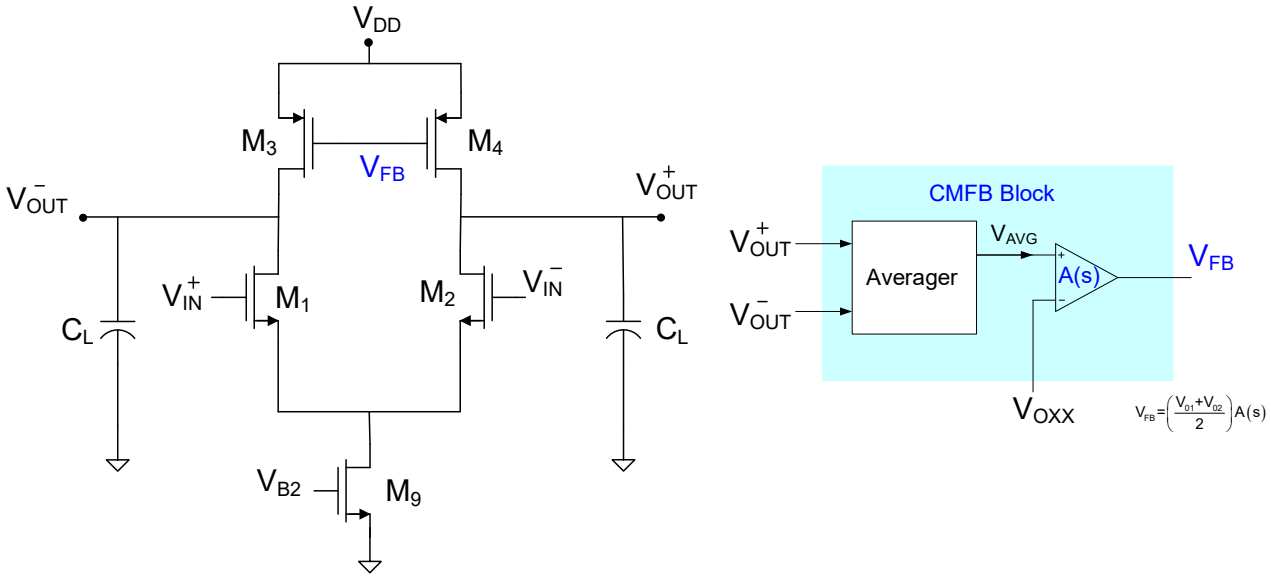
This circuit has 3 different natural common-mode inputs:

$$V_{B1},\ V_{B2},\ \frac{V_1 + V_2}{2}$$

V_{B1} or V_{B2} (or possibly both in some way) are the inputs for CMFB

Can it be argued that it is still a single-stage common-mode circuit irrespective of which common-mode input is used and thus compensation of the common-mode circuit will not be required?

Does this amplifier need compensation?



The CMFB path from V_{FB} back to V_{FB} is a two-stage feedback amplifier comprised of the common-mode gain of the basic 5T circuit from V_{FB} to V_{OUT} and the common-mode gain from V_{OUT} to V_{FB}

This amplifier needs compensation (of the CMFB path) even if the basic amplifier is single-stage

The overall amplifier including the β amplifier for the differential feedback path should be considered when compensating the CMFB circuit

If a second-stage is added to the 5T op amp, the compensation network for the differential stage may also provide the needed compensation for the CMFB path

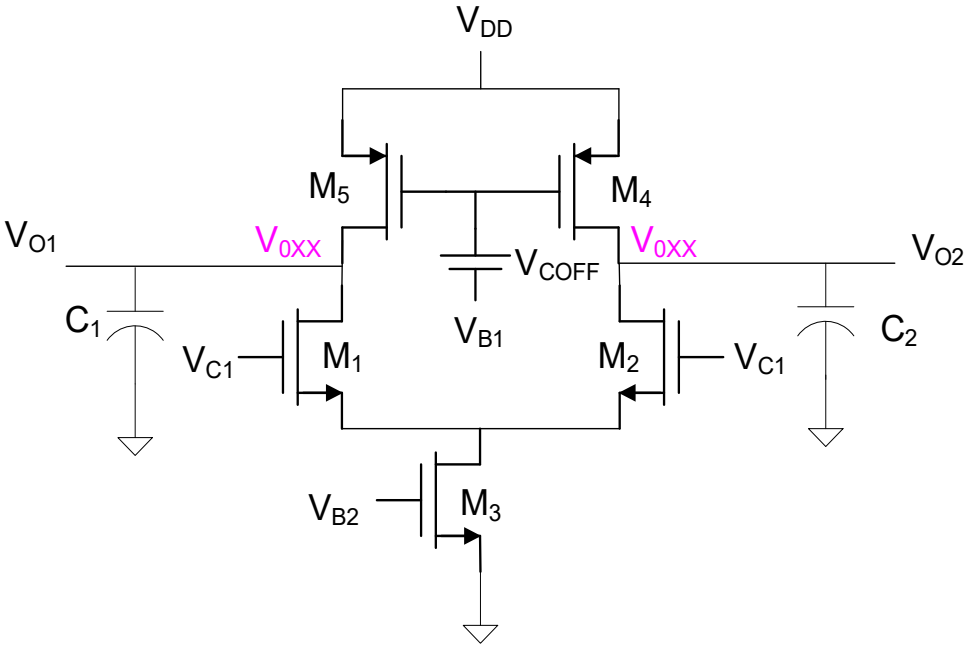
Common-Mode and Difference-Mode Issues

Overall poles are the union of the common-mode and difference mode poles

Separate analysis generally required to determine common-mode and difference-mode performance

Some amplifiers will need more than one CMFB

Common-mode offset voltage



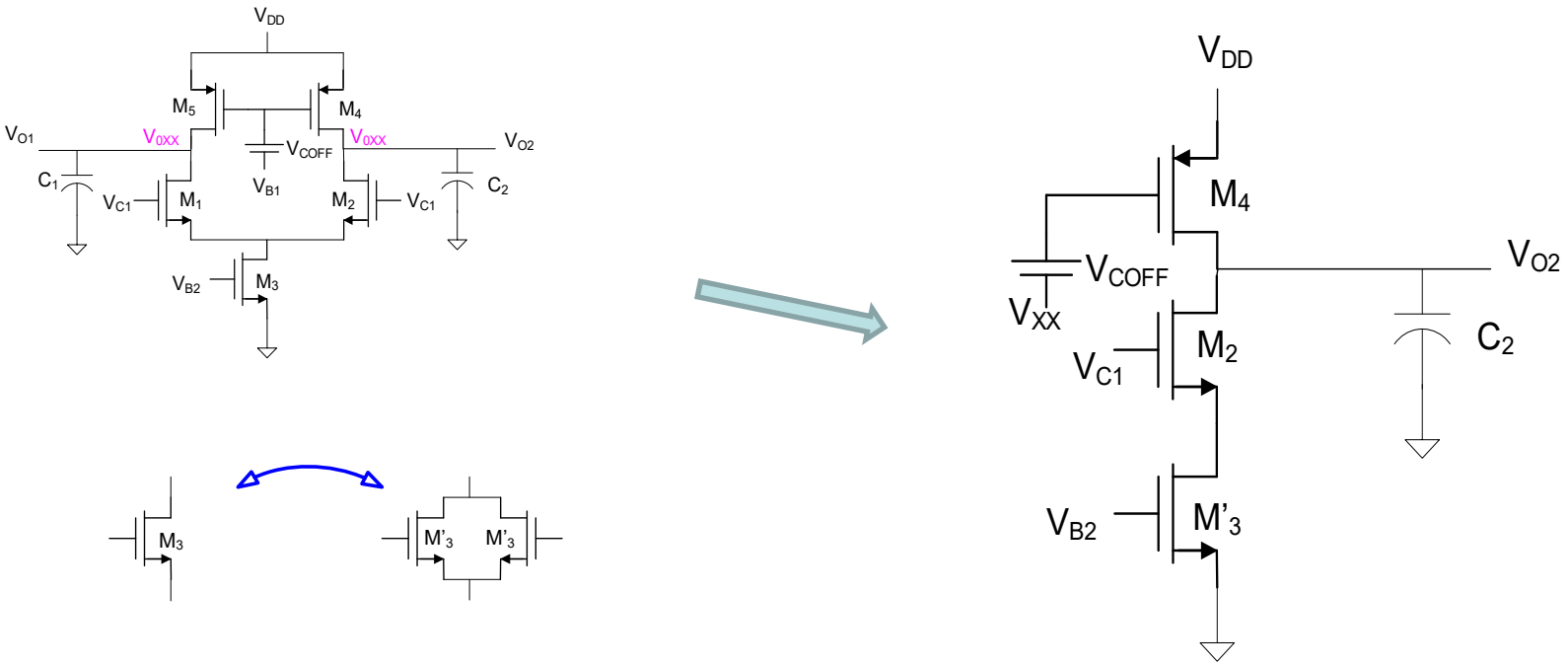
Assume ideally V_{B1} will provide the desired value for V_{OXX}

Definition: The common-mode offset voltage is the voltage that must be applied to the biasing node at the CMFB point to obtain the desired operating point at the stabilization node

Note: Could alternately define common-mode offset relative to V_{B2} input if CMFB to M_3

Common-mode offset voltage

Consider again the Common-mode half circuit



There are three common-mode inputs to this circuit !

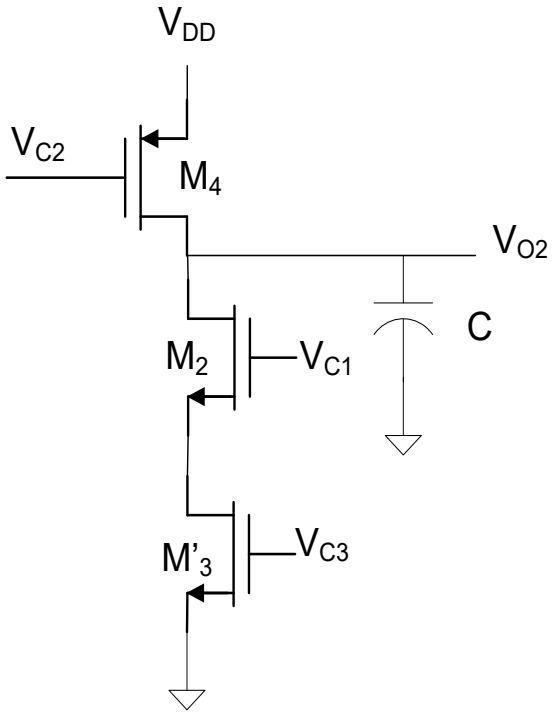
The common-mode signal input is distinct from the input that is affected by V_{COFF}

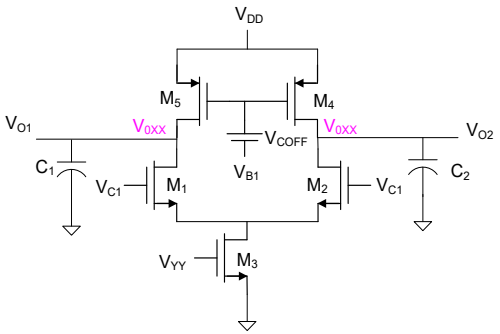
The gain from the common-mode input where V_{FB} is applied may be critical !

How do the poles from the three different CM inputs relate to each other?

They are the same!!

Common-mode gains





$$A_{COM} = \frac{V_{02}}{V_{C1}} \cong -\frac{g_{02}+g_{03}/2}{sC+g_{04}}$$

$$A_{COM2} = \frac{V_{02}}{V_{C2}} \cong -\frac{g_{m4}}{sC+g_{04}}$$

$$A_{COM3} = \frac{V_{02}}{V_{C3}} \cong -\frac{g_{m3}/2}{sC+g_{04}}$$

$$A_{COM0} \cong -\frac{g_{02}+g_{03}/2}{g_{04}} = -\frac{\lambda I_T}{\lambda I_T/2} = -\frac{1}{2}$$

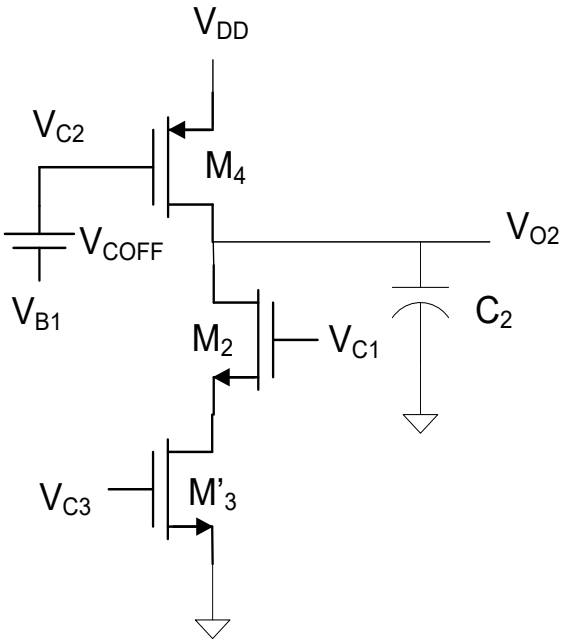
$$A_{COM20} \cong -\frac{g_{m4}}{g_{04}} = -\frac{2I_T/V_{EB4}}{\lambda I_T/2} = -\frac{4}{V_{EB4}\lambda}$$

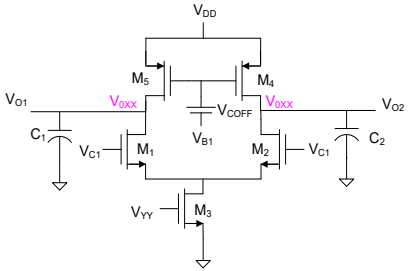
$$A_{COM30} \cong -\frac{g_{m3}/2}{g_{04}} = -\frac{\frac{2I_T}{V_{EB3}}/2}{\lambda I_T/2} = -\frac{2}{\lambda V_{EB3}}$$

Although the common-mode gain A_{COM0} is very small, A_{C0M20} is very large! (but can be reduced by partitioning M_4)

Shift in V_{02Q} from V_{OXX} is the product of the common-mode offset voltage and A_{COM20}

Effect of common-mode offset voltage





$$A_{COM20} \cong -\frac{4}{V_{EB5}\lambda}$$

$$\Delta V_{02} = A_{COM20} V_{COFF}$$

How much change in V_{02} is acceptable? (assume e.g. 50mV)

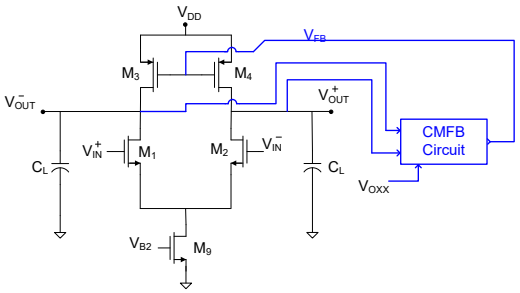
How big is V_{COFF}? (similar random expressions for V_{OS}, assume, e.g. 25mV)
(that due to process variations even larger)

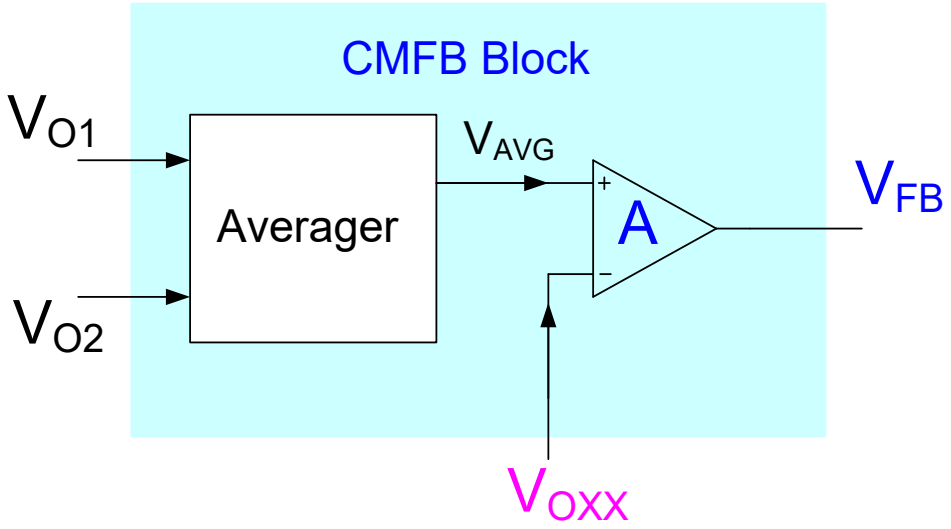
How big is A_{COM20}? (if λ=.01, V_{EB}=.2, A_{COM20}=2000)

If change in V_{02} is too large, CMFB is needed

(50mV >? 2000x25mV)

How much gain is needed in the CMFB amplifier?



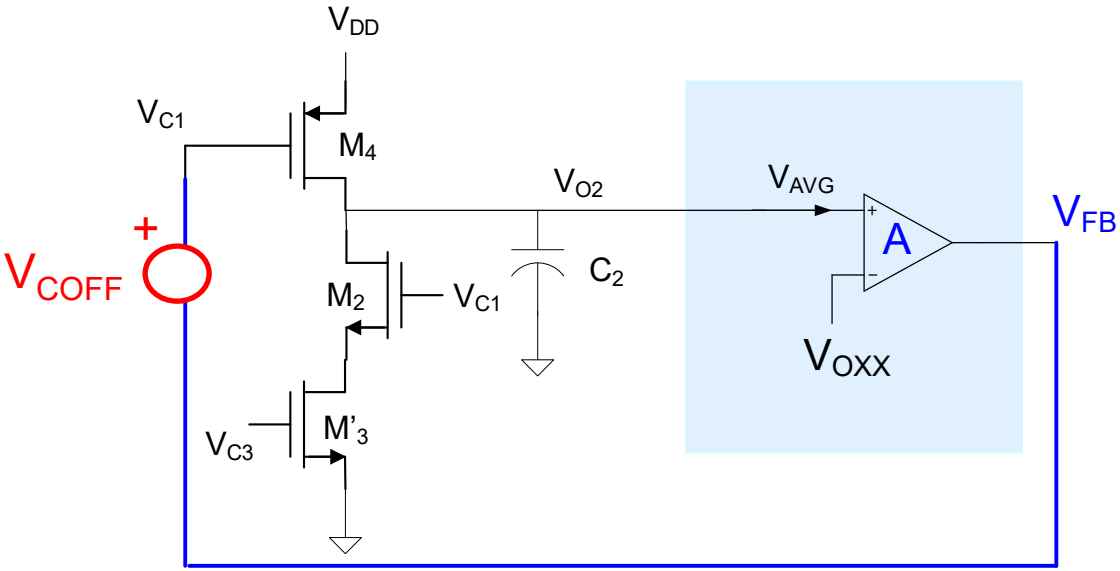


CMFB must compensate for V_{COFF}

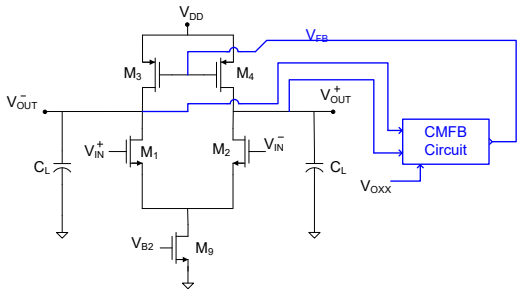
Want to guarantee $\left|V_{02Q}-V_{0XX}\right| < \Delta V_{OUT\text{-}ACCEPTABLE}$

This is essentially the small-signal output with a small-signal input of V_{COFF}

How much gain is needed in the CMFB amplifier?



The CMFB Loop



Want to guarantee

$$\left|V_{02Q}-V_{0XX}\right| < \Delta V_{OUT\text{-}ACCEPTABLE}$$

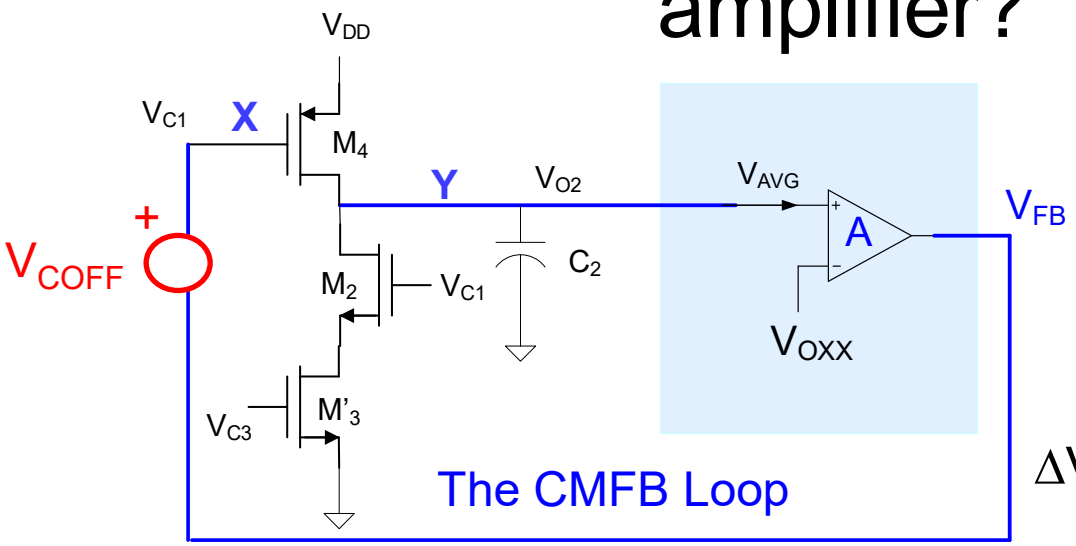
Do a small-signal analysis, only input is V_{COFF}

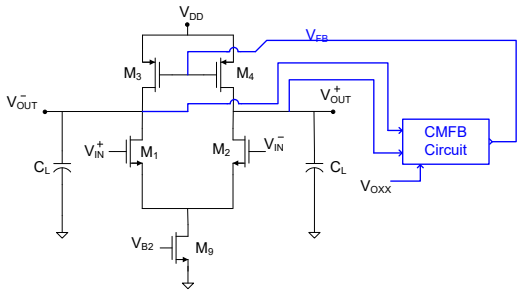
$$V_{02}=\left(V_{02}A+V_{COFF}\right)A_{COM2}$$

$$V_{02}=V_{COFF}\frac{A_{COM2}}{1-AA_{COM2}}$$

$$\Delta V_{0UT\text{-}ACCEPTABLE}=V_{COFF}\frac{A_{COM2}}{1-AA_{COM2}}$$

How much gain is needed in the CMFB amplifier?





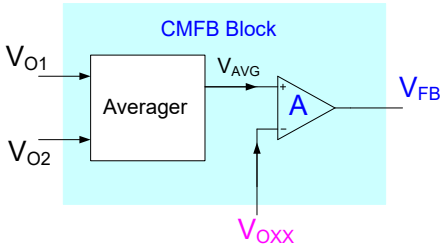
$$\Delta V_{0UT\text{-}ACCEPTABLE} = V_{COFF} \frac{A_{COM2}}{1 - AA_{COM2}}$$

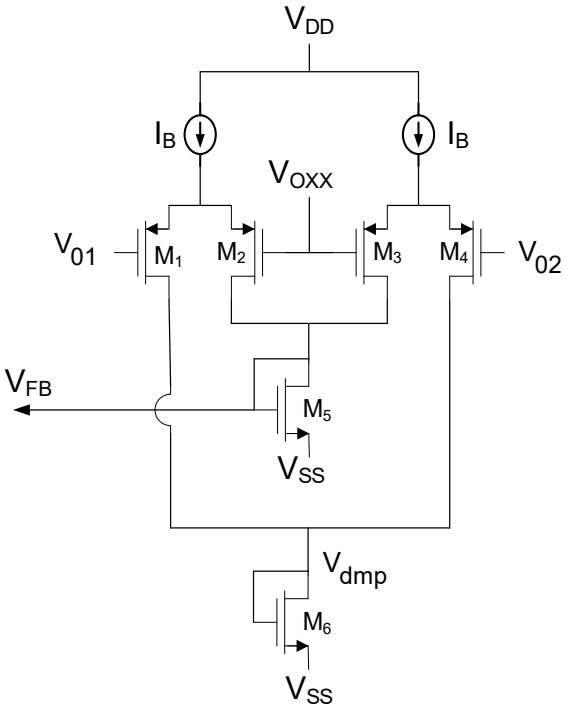
- Node **Y** is common to both differential feedback loop and CMFB loop
- This does not require a particularly large gain
- This is the loop that must be compensated since A and A_{COMP2} will be frequency dependent
- Miller compensation capacitor for compensation of differential loop will often appear in shunt with C_2
- Can create this “half-circuit” loop (without CM inputs on a fully differential structure) for simulations
- Results extend readily to two-stage structures with no big surprises
- Capacitances on nodes **X** and **Y** as well as compensation C in A amplifier (often same as capacitor on **Y** node) create poles for CMFB circuit
- Reasonably high closed-loop CMFB bandwidth needed to minimize shifts in output due to high-frequency common-mode noise

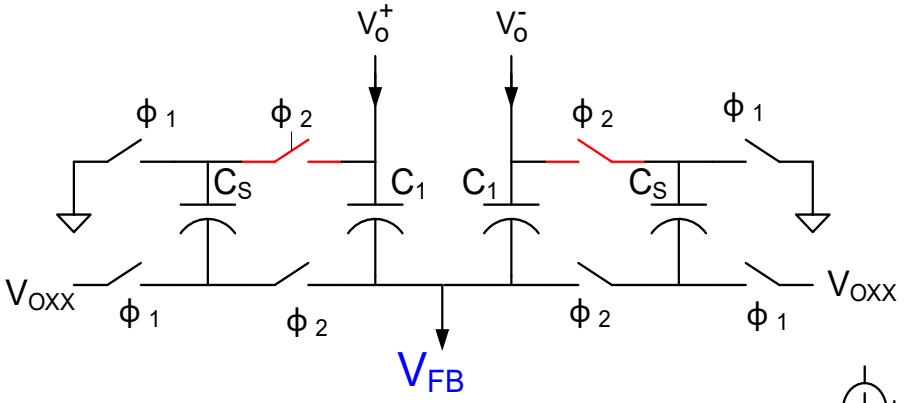
Compensation of CMFB loop will affect differential compensation if C_2 needs to be changed

CMFB Circuits

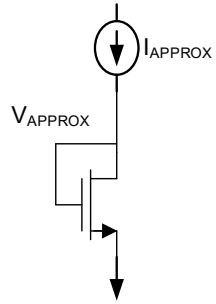
- Several (but not too many) CMFB blocks are widely used
- Can be classified as either continuous-time or discrete-time





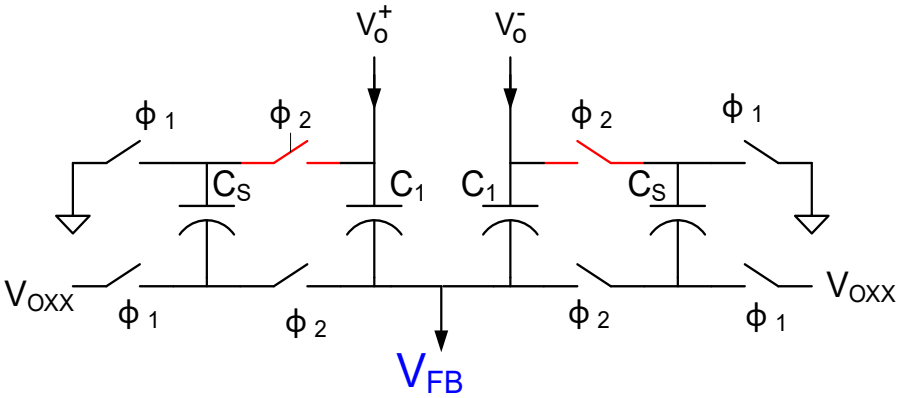


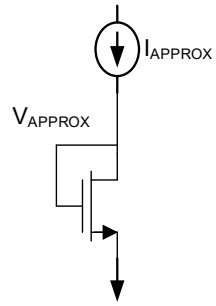
C_S small compared to C_1



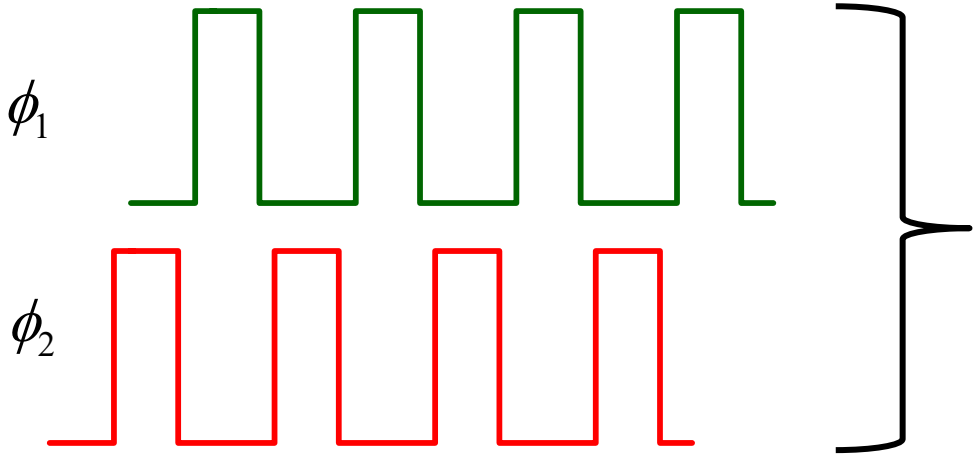
- V_{OXX} generated by simple bias generator
- φ_1 and φ_2 are complimentary non-overlapping clocks that run continuously
- At this point, think of V_{dmp} as a place to "dump" the current from the diff pairs
- But V_{dmp} does contain the same information as V_{FB}, only of opposite sign!

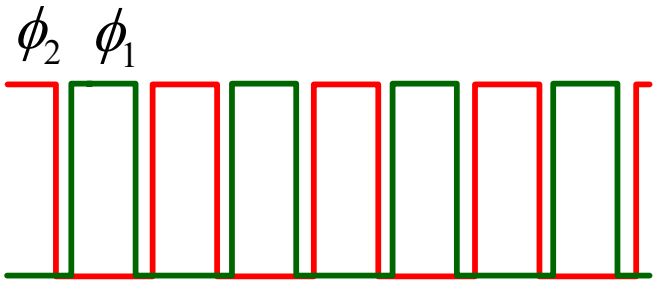
CMFB Circuits





φ_1 and φ_2 are complimentary non-overlapping clocks that run continuously

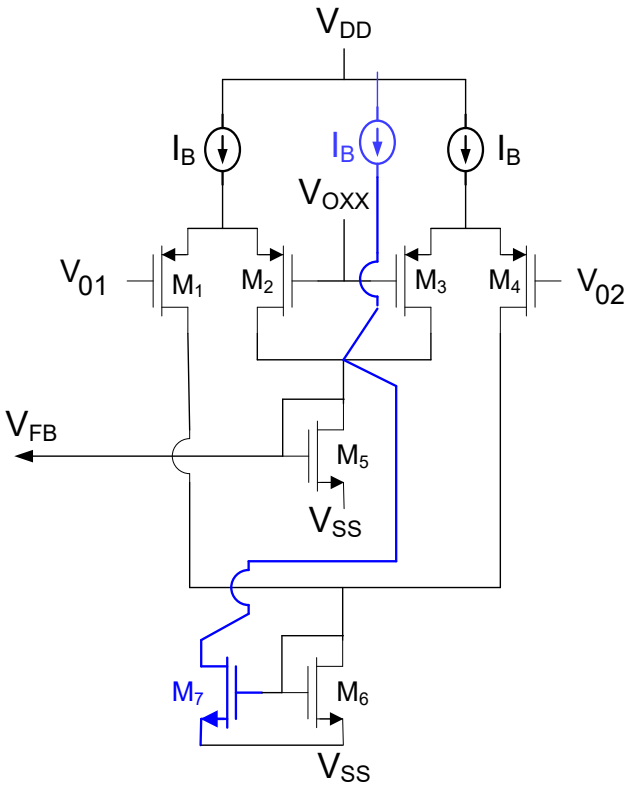


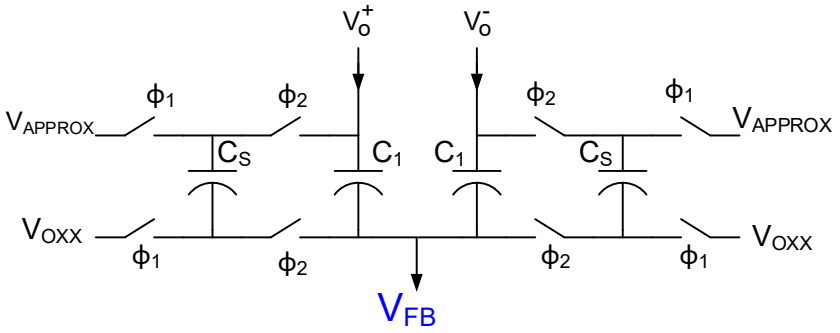


- non-overlap of φ_1 and φ_2 is critical but frequency is not critical
- Could even have 25% or less duty cycle to guarantee non-overlap
- φ_1 and φ_2 run asynchronously with respect to the op amp

CMFB Circuits

Several (but not too many) CMFB circuits exist
Can be classified as either continuous-time or discrete-time





Circuit in blue can be added to double CMFB gain

Stay Safe and Stay Healthy !

End of Lecture 23